Jones/Cujo 2.0 (UP6/7) BLOCK DIAGRAM

01

PCB STACK UP
6L Dis.

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

CPU
Auburndale 35W
Clarksfield 45W
PAGE 3~6

DDRIII-SODIMM1 PAGE 12 — DDRIII 800/1066 MT/s, 1333MT/s CFD only
DDRIII-SODIMM2 PAGE 13 — DDRIII 800/1066 MT/s, 1333MT/s CFD only

PCI-Express 16X → nVIDIA N10M-GE / N10P-GE 128 Bit, PAGE 14~20, 969p (27MHz)
- HDMI CON PAGE 22
- CRT PAGE 22
- Dual Link → LCD CONN PAGE 21

DMI LINK (32.768KHz, 25MHz)

PCH
Ibex-M
PAGE 7~11

- SATA - HDD PAGE 31 — SATA0 150MB
- SATA - CD-ROM PAGE 31 — SATA1 150MB
- SATA - 2ndHDD PAGE 31 — SATA4 150MB
- E-SATA PAGE 30 — SATA5 150MB
- Accelerometer LIS3LV02DL PAGE 25 — SMBUS

CLOCK GEN 9LRS3197 PAGE 2 (14.318MHz)

USB2.0 (4,7,10,11)
- USB2.0 Ports X4 PAGE 30 (0,1,8,9)
- BlueTooth PAGE 30 (5)
- Webcam PAGE 30 (3)
- Fingerprint PAGE 30 (2)
- Mini PCI-E Card x2 / Express Card x1 / Cable Docking x1

PCI-E (24.576MHz)
- Mini PCI-E Card WWAN/TV PAGE 34 (X1)
- Mini PCI-E Card Wireless LAN PAGE 34 (X1)
- LAN Realtek RTL8111DL GigaLAN PAGE 27 (X1) — 25MHz → RJ45 PAGE 27
- Express Card PAGE 31 (X1)
- JMICRO 380 PAGE 23 (X1)
  - IEEE1394 PAGE 23
  - Memory CardReader PAGE 23

Azalia
- Analog IDT92HD75B3 PAGE 24
  - AUDIO Amplifier TPA6047A4 PAGE 25
  - AUDIO Amplifier TPA3007D1 PAGE 26
- microphone PAGE 24
- Audio Jacks (Phone/ MIC) PAGE 24
- Jack to Speaker PAGE 25
- Jack to Sub-Woofer PAGE 26

ONFI
- Braidwood PAGE 33
- SPI PAGE 7
- MDC CONN PAGE 32

LPC

ENE KBC
KB3926 D2
PAGE 29 (32.768KHz)
- Keyboard PAGE 31 / Touch Pad PAGE 29
- Capacitive Sense SW PAGE 32
- GMT G9931P1U FAN PAGE 32
- SPI PAGE 29

Cable Docking PAGE 32
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

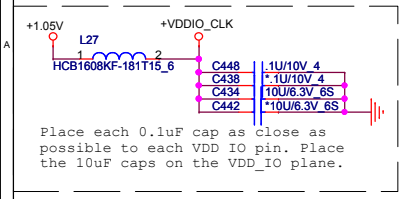
- SYSTEM POWER RT8206B PAGE 35
- VCCP +1.1VTT(RT8208A) AND PCH 1.05V(RT8204) PAGE 36
- CPU CORE ISL6251A PAGE 41
- VGACORE(1.025V) RT8208A PAGE 38
- DDR III SMDDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 39
- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 40

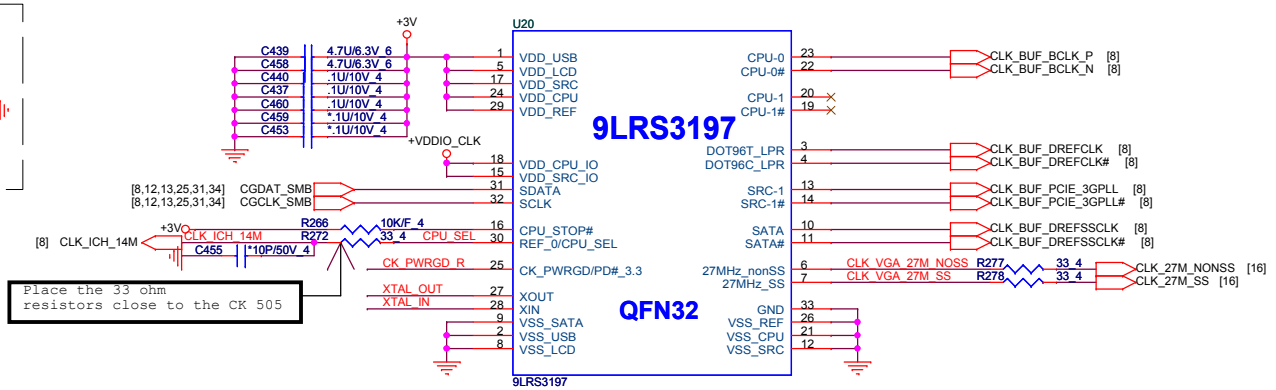
NB5

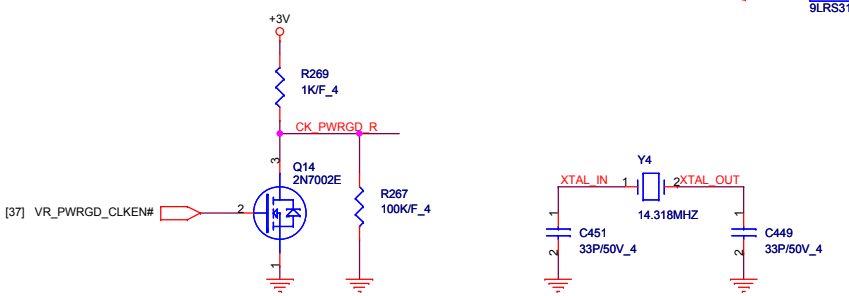
PROJECT : UP67
Quanta Computer Inc.

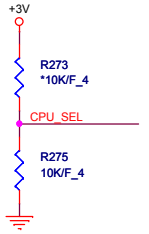
Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Monday, October 26, 2009 Sheet 1 of 45



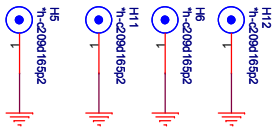




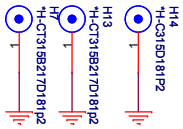


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

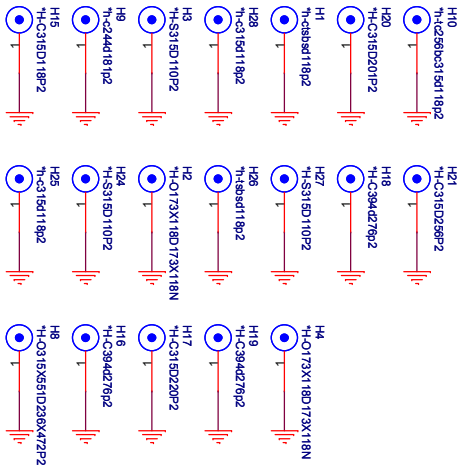
CPU bracket Hole.



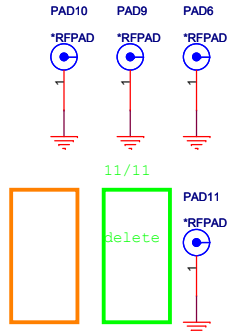
VGA bracket Hole.



M/B Screw Hole



RF PAD

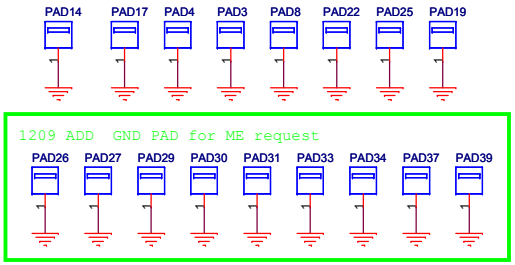


5/18 PV :delete PAD12

ME PAD

Routed spring

ME-Ground Pad



[3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK & Screw Holes	1A

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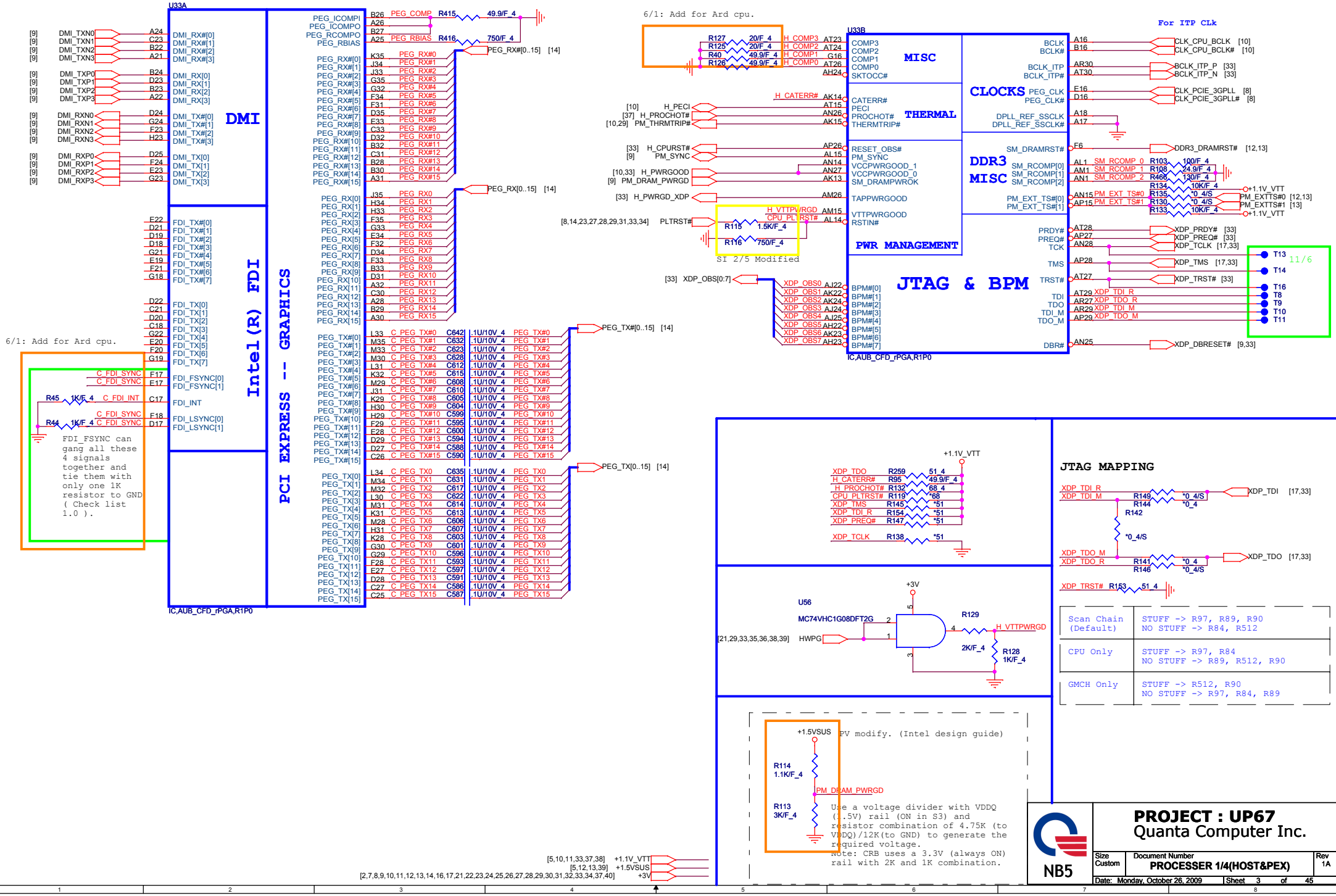
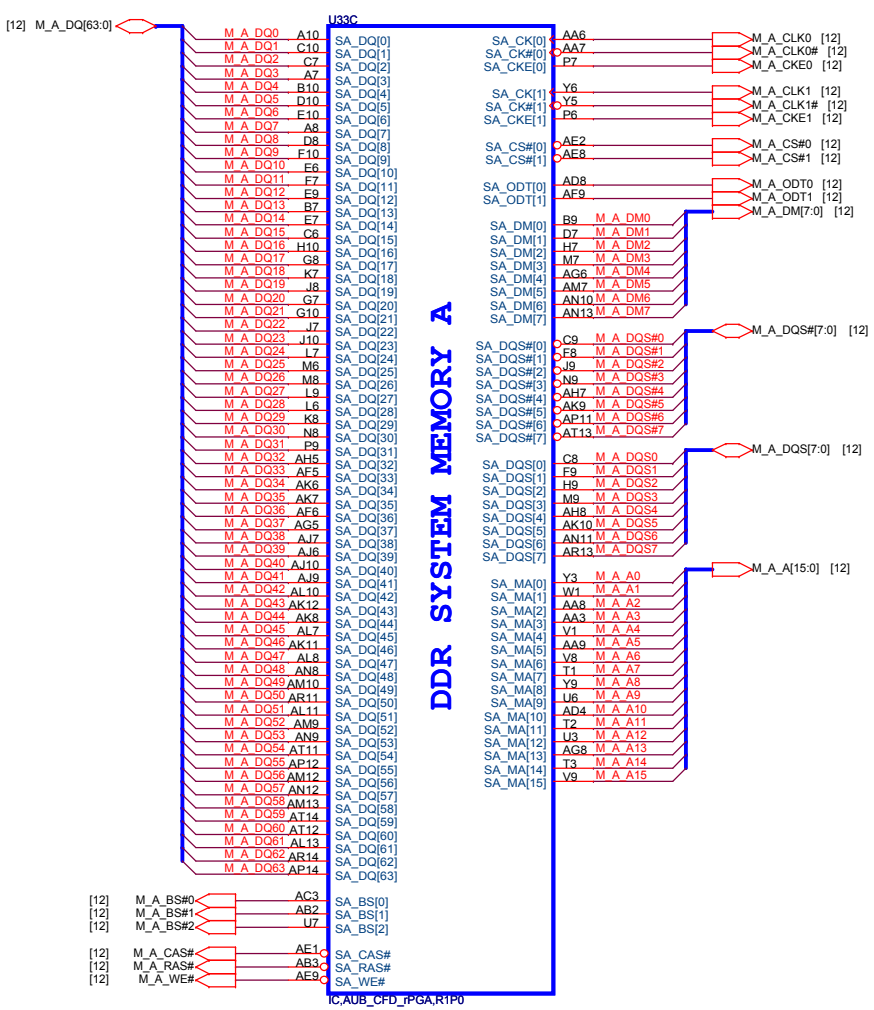
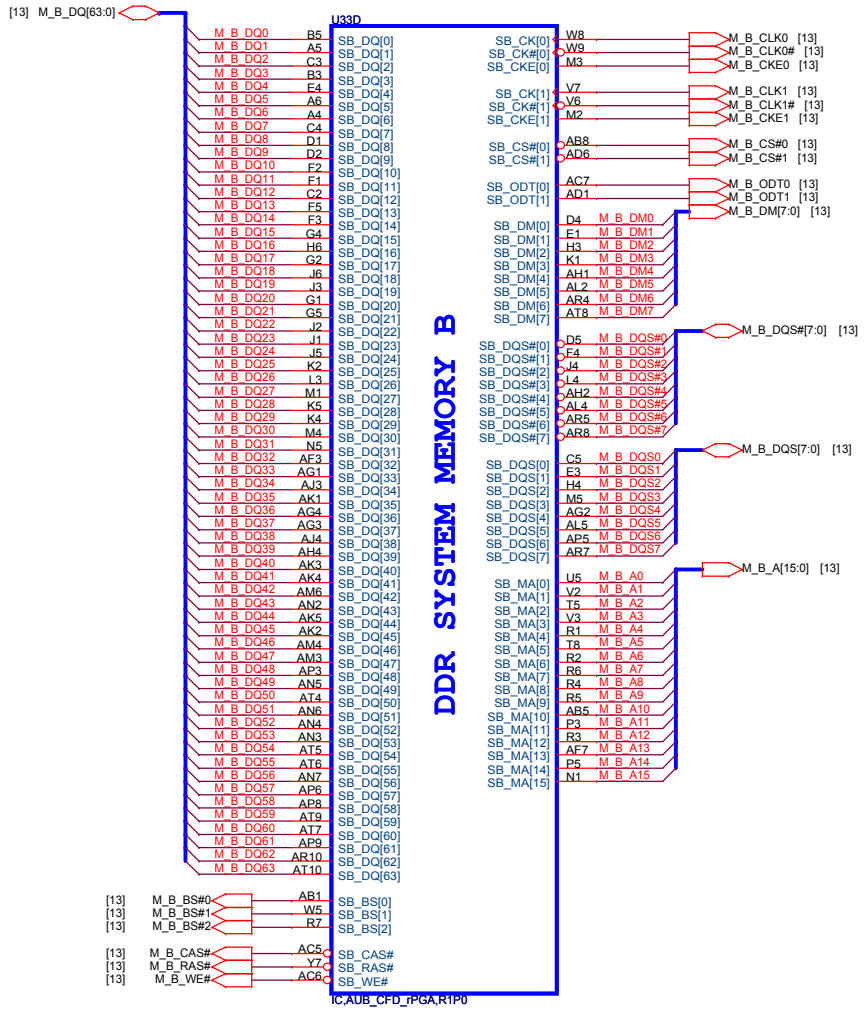
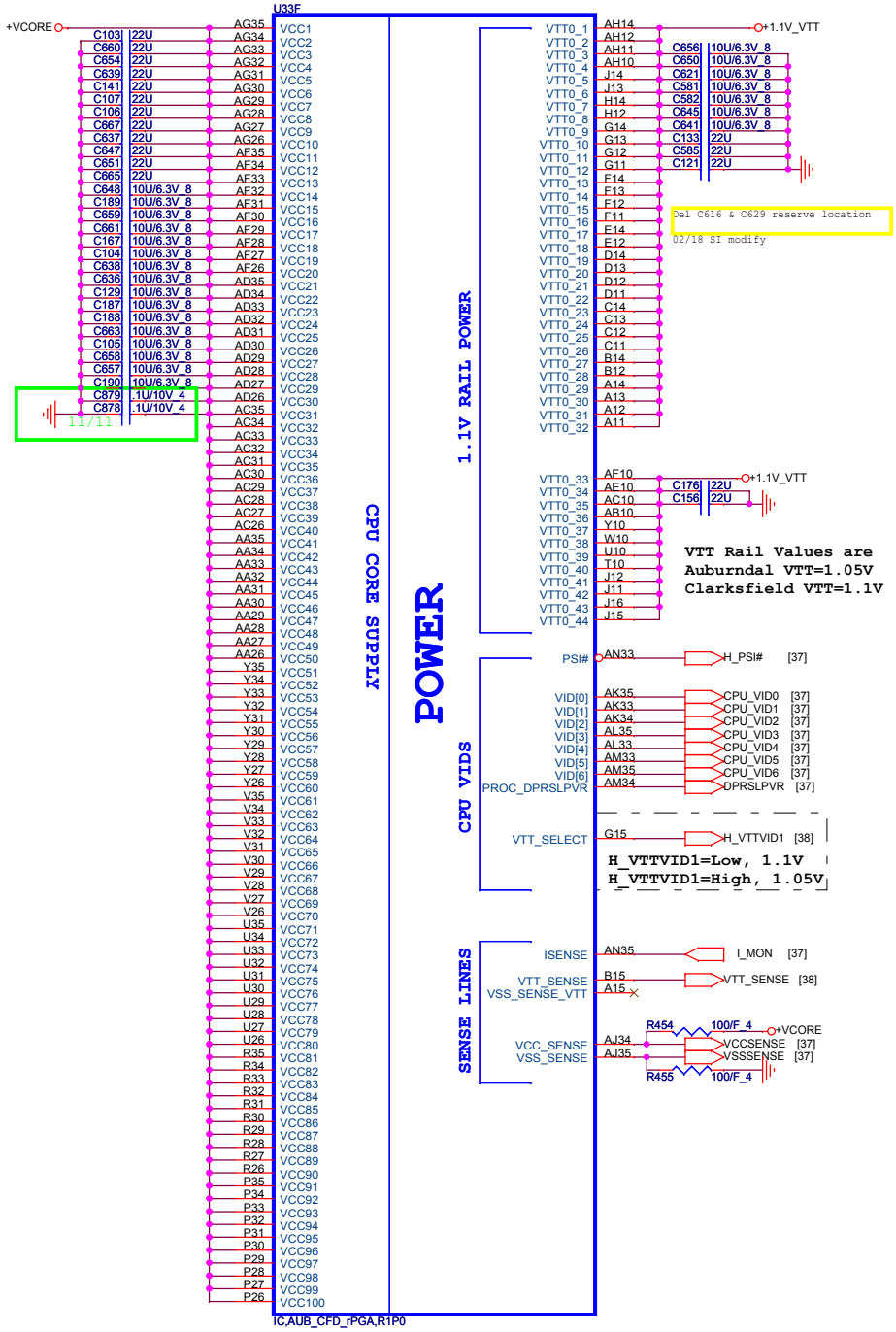

U33A
DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
IC,AUB_CFD_rPGA,R1P0
6/1: Add for Ard cpu.
FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).
U33B
MISC
THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
IC,AUB_CFD_rPGA,R1P0
SI 2/5 Modified
For ITP CLk
JTAG MAPPING
Scan Chain (Default) STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only STUFF -> R512, R90 NO STUFF -> R97, R84, R89
PV modify. (Intel design guide)
Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.
PROJECT : UP67
Quanta Computer Inc.
NB5
PROCESSER 1/4(HOST&PEX)
Size Custom
Rev 1A
Date: Monday, October 26, 2009
Sheet 3 of 45

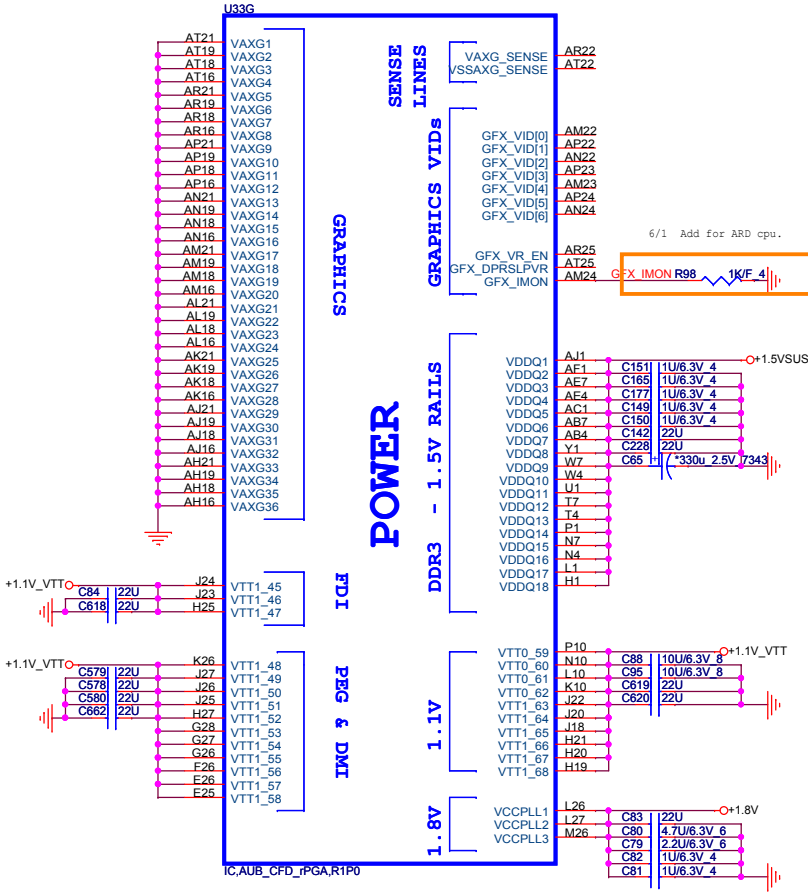
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

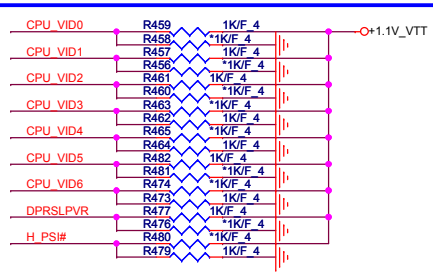




NB5	**PROJECT : UP67** Quanta Computer Inc.	
Size: Custom	Document Number: **PROCESSER 2/4(DDR)**	Rev: 1A
Date: Monday, October 26, 2009	Sheet 4 of 45	







[37] +VCORE
[3,10,11,33,37,38] +1.1V_VTT
[3,12,13,39] +1.5VSUS
[10,11,33,36,40] +1.8V

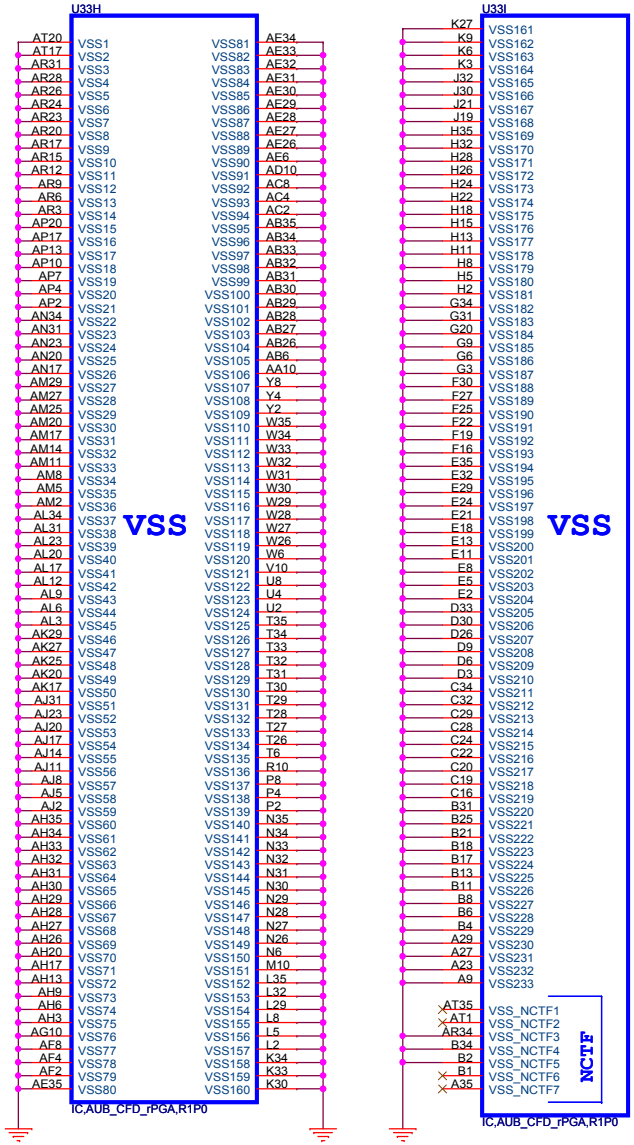
NB5

PROJECT : UP67
Quanta Computer Inc.

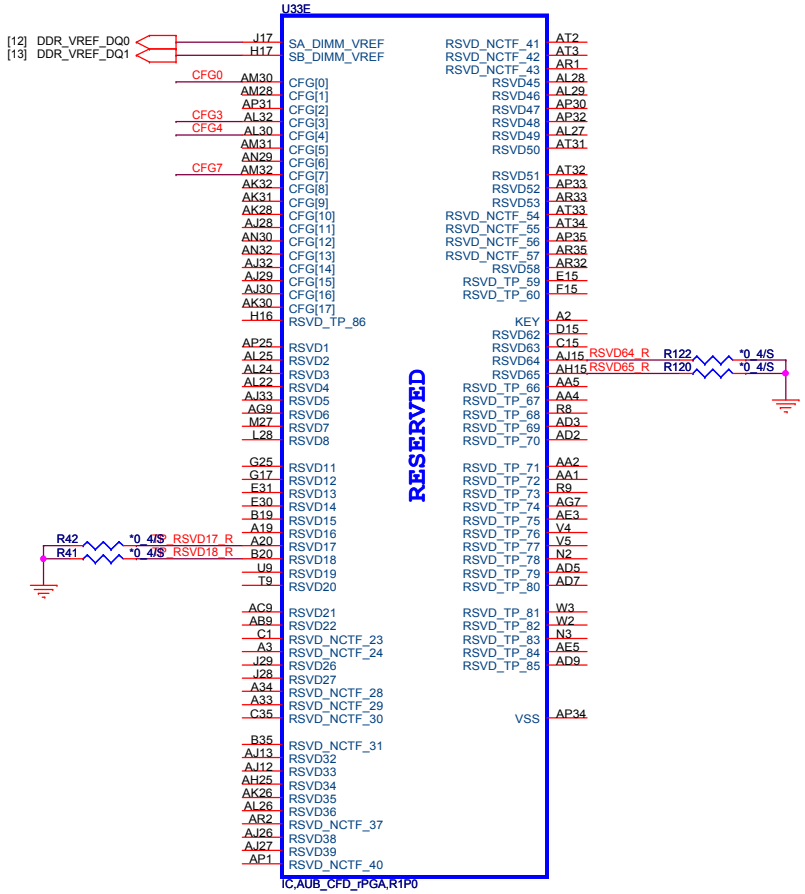
Size	Document Number	Rev
Custom	PROCESSER 3/4(POWER)	1A

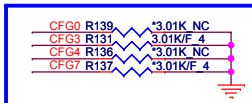
Date: Monday, October 26, 2009 Sheet 5 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

NB5

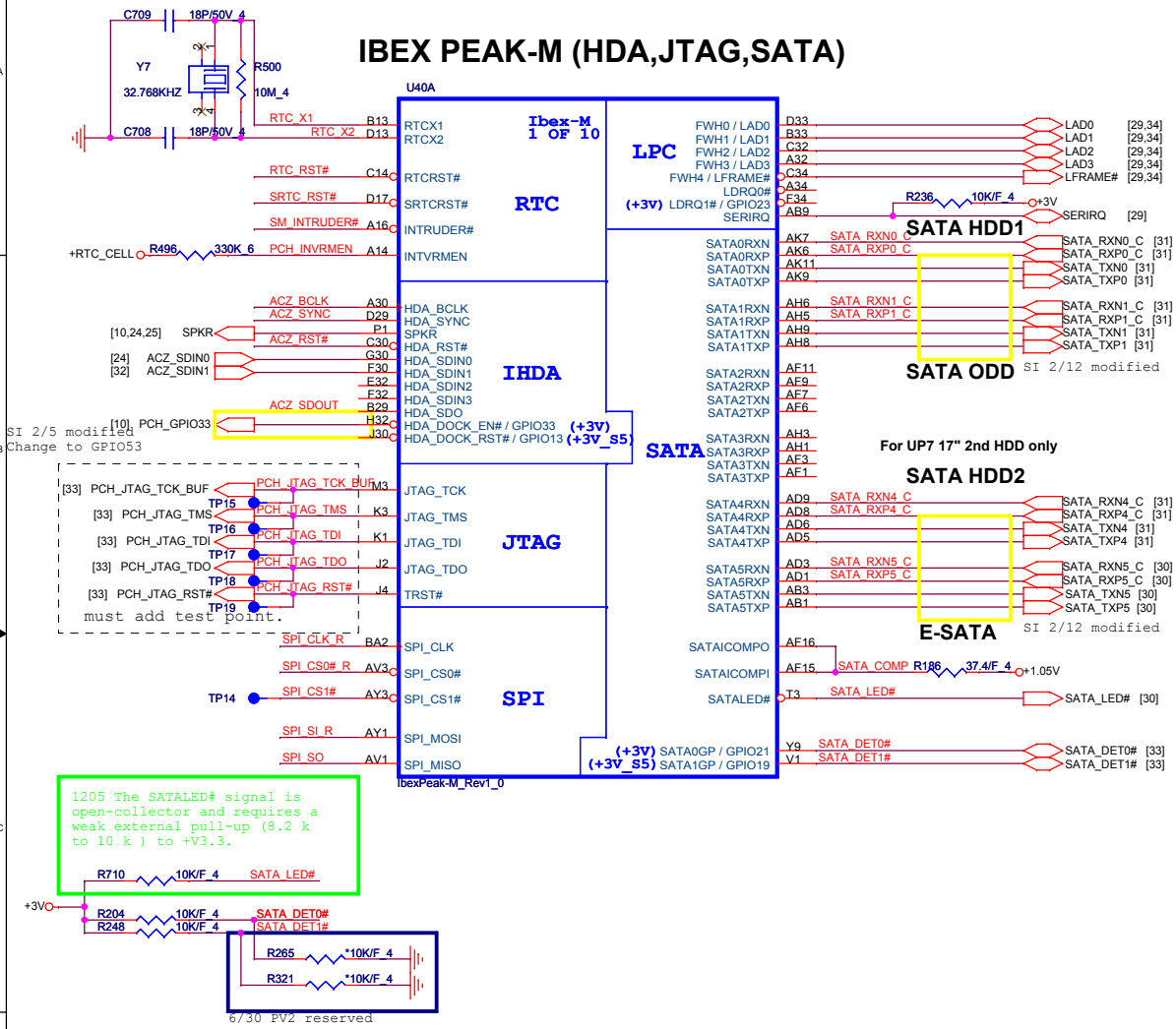
PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	1A

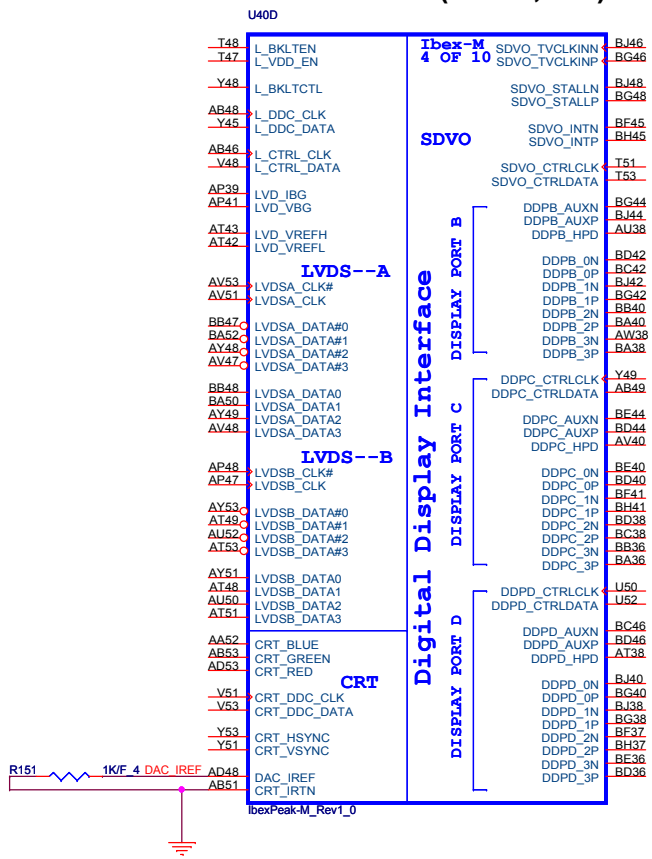
Date: Monday, October 26, 2009 Sheet 6 of 45

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

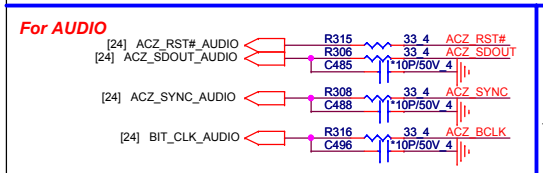
IBEX PEAK-M (HDA,JTAG,SATA)



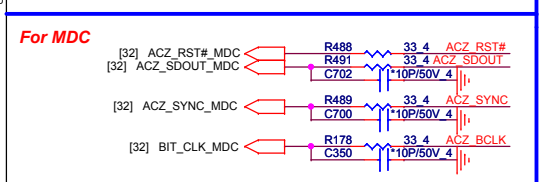
IBEX PEAK-M (LVDS,DDI)



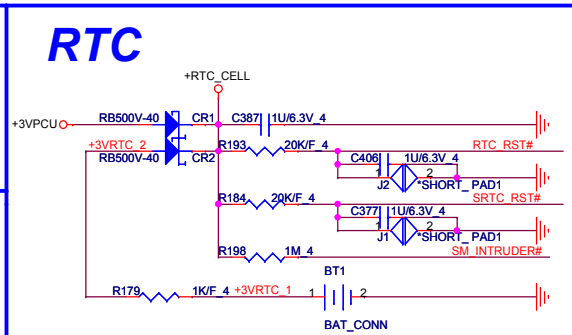
For AUDIO



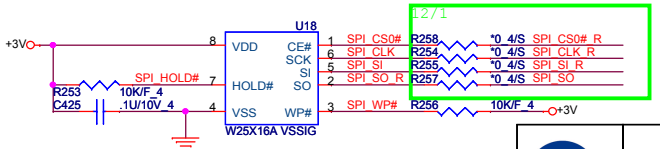
For MDC



RTC



2M byte SPI ROM for ME & Bios



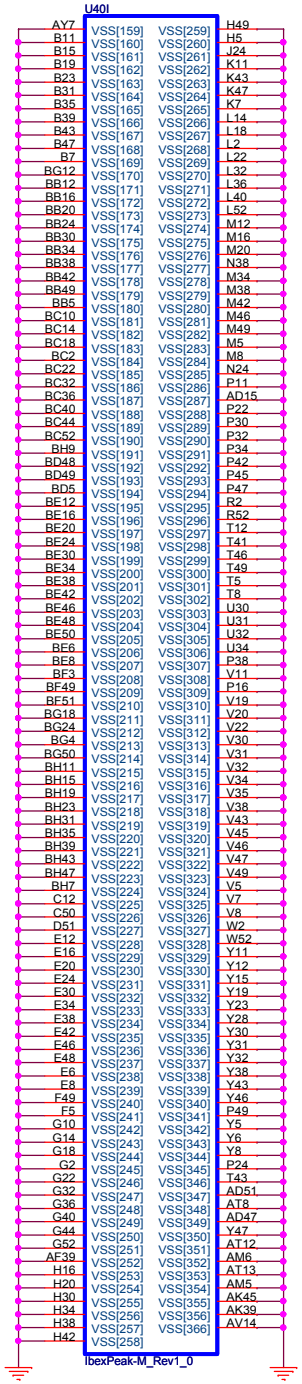
Socket: DG008000031
MXIC AKE38FP0Z00
WINBOND AKE38ZP0N01
SI 2/17 modified

PROJECT : UP67
Quanta Computer Inc.

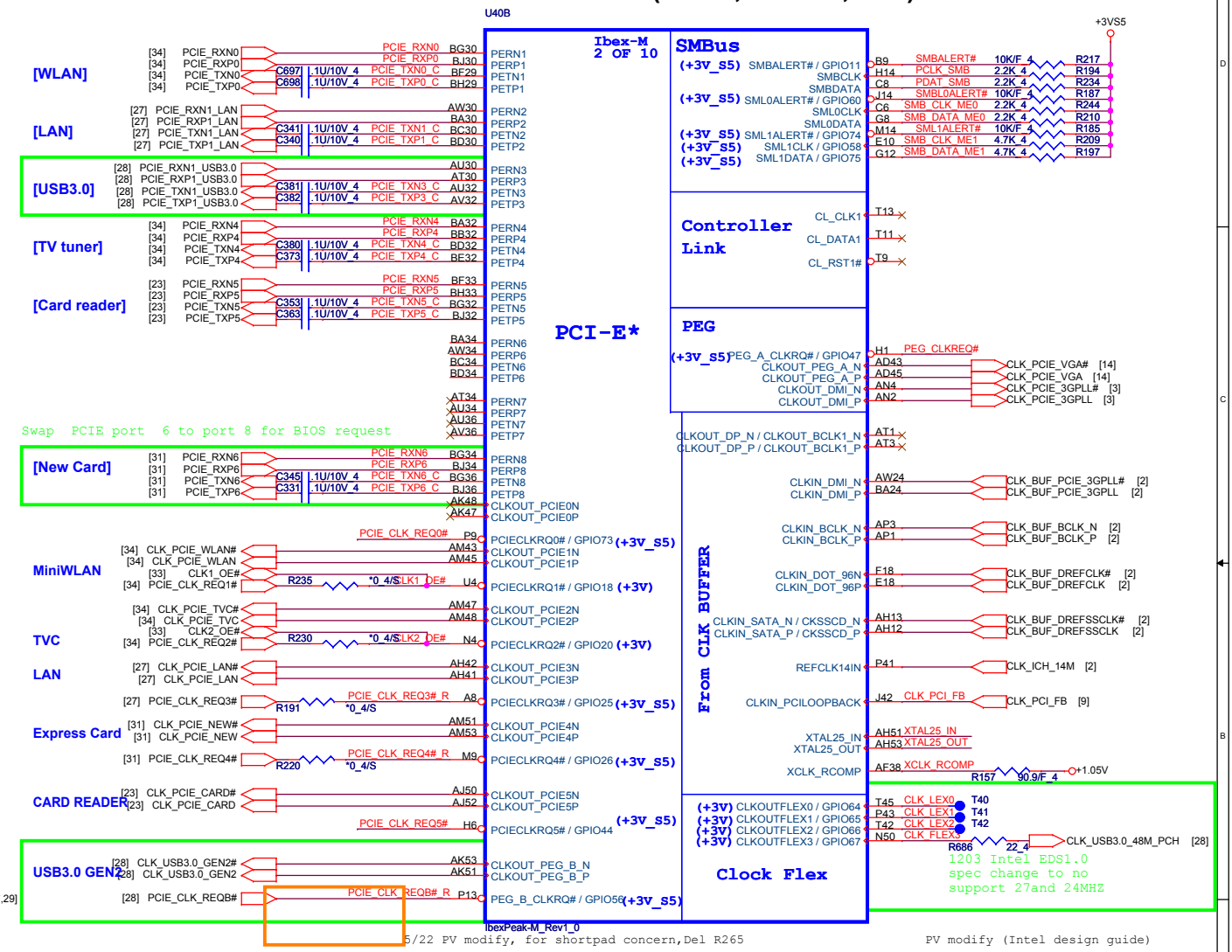
Size	Document Number	Rev
Custom	PCH 2/6 (SATA,HDA,LPC)	1A
Date: Monday, October 26, 2009	Sheet 7 of 45	

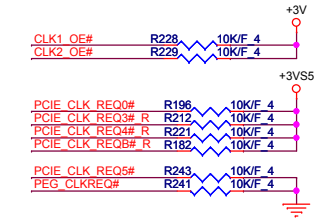
NB5

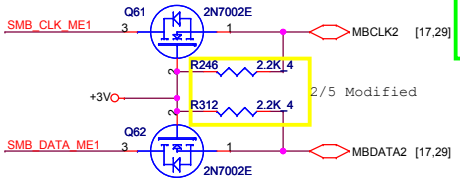
IBEX PEAK-M (GND)

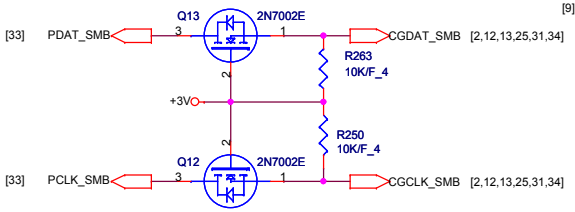


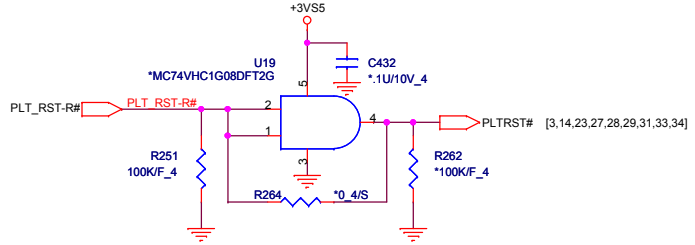
IBEX PEAK-M (PCI-E,SMBUS,CLK)





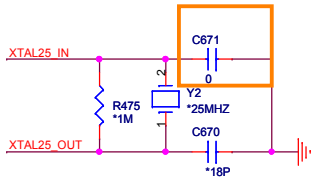






5/22 PV modify, for shortpad concern,Del R265

PV modify (Intel design guide)



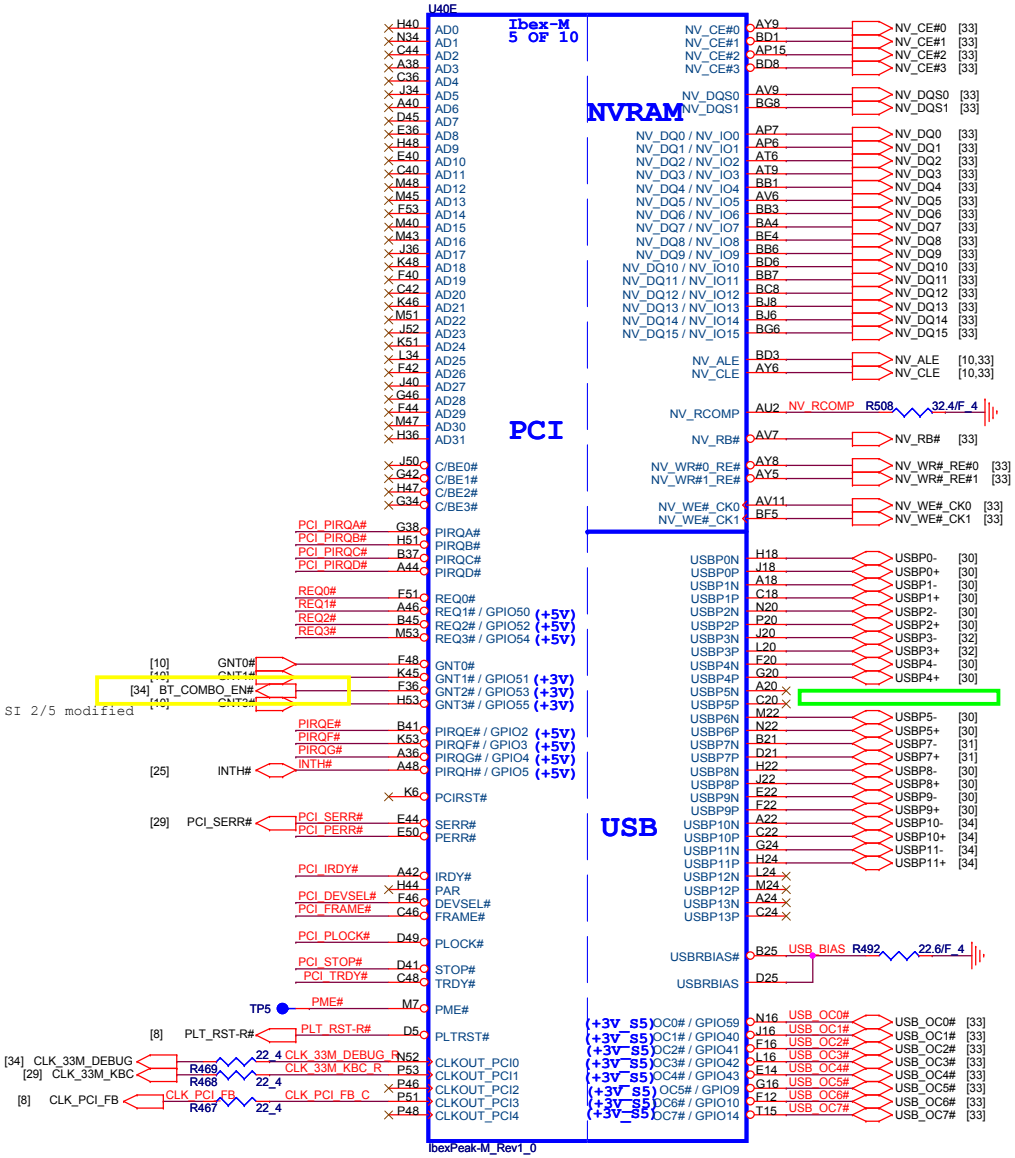
[2,7,9,11,14,15,16,28,29,33,36] +1.05V
[2,3,7,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,12,13,21,29,30,31,32,34,35,36,38,40,41] +3VPCU

NB5	**PROJECT : UP67** Quanta Computer Inc.	
Size: Custom	Document Number: PCH 3/6 (PCI,ONFI,USB,CK)	Rev: 1A
Date: Monday, October 26, 2009	Sheet 8 of 45	

IBEX PEAK-M (PCI,USB,NVRAM)

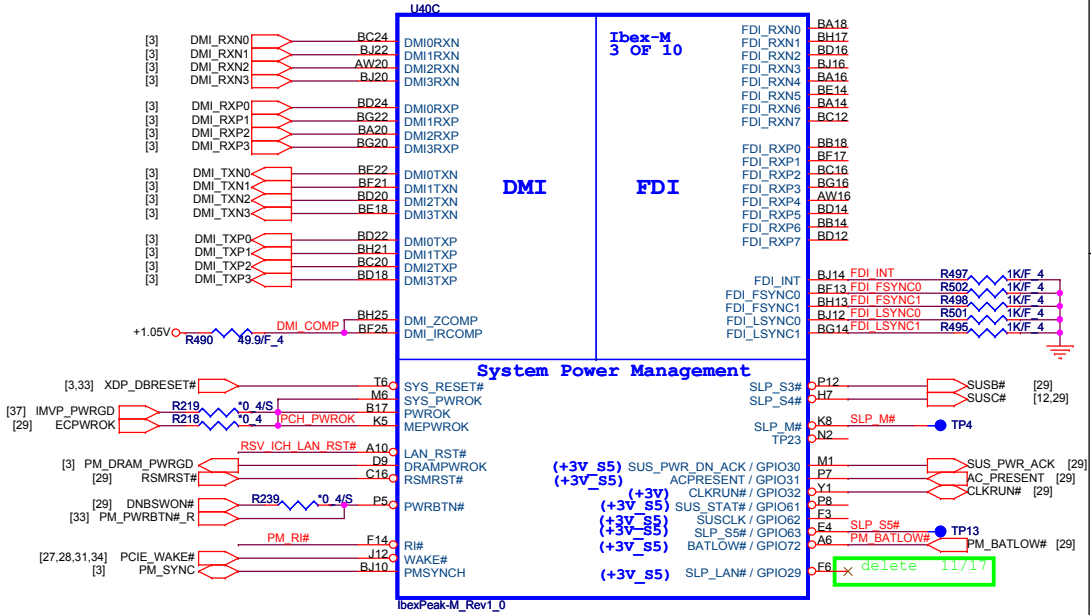
IBEX PEAK-M (DMI,FDI,GPIO)

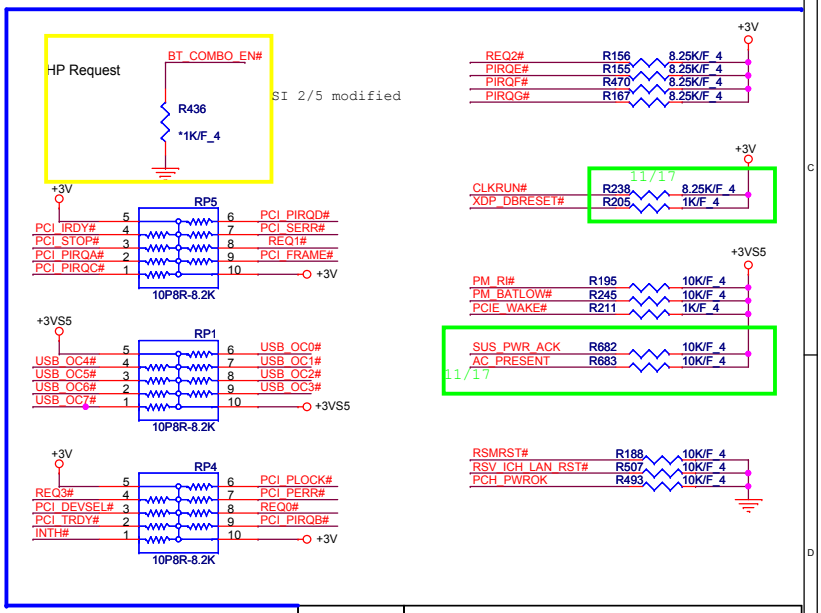
09



SI 2/5 modified

1209 swap to port 6 from BIOS request





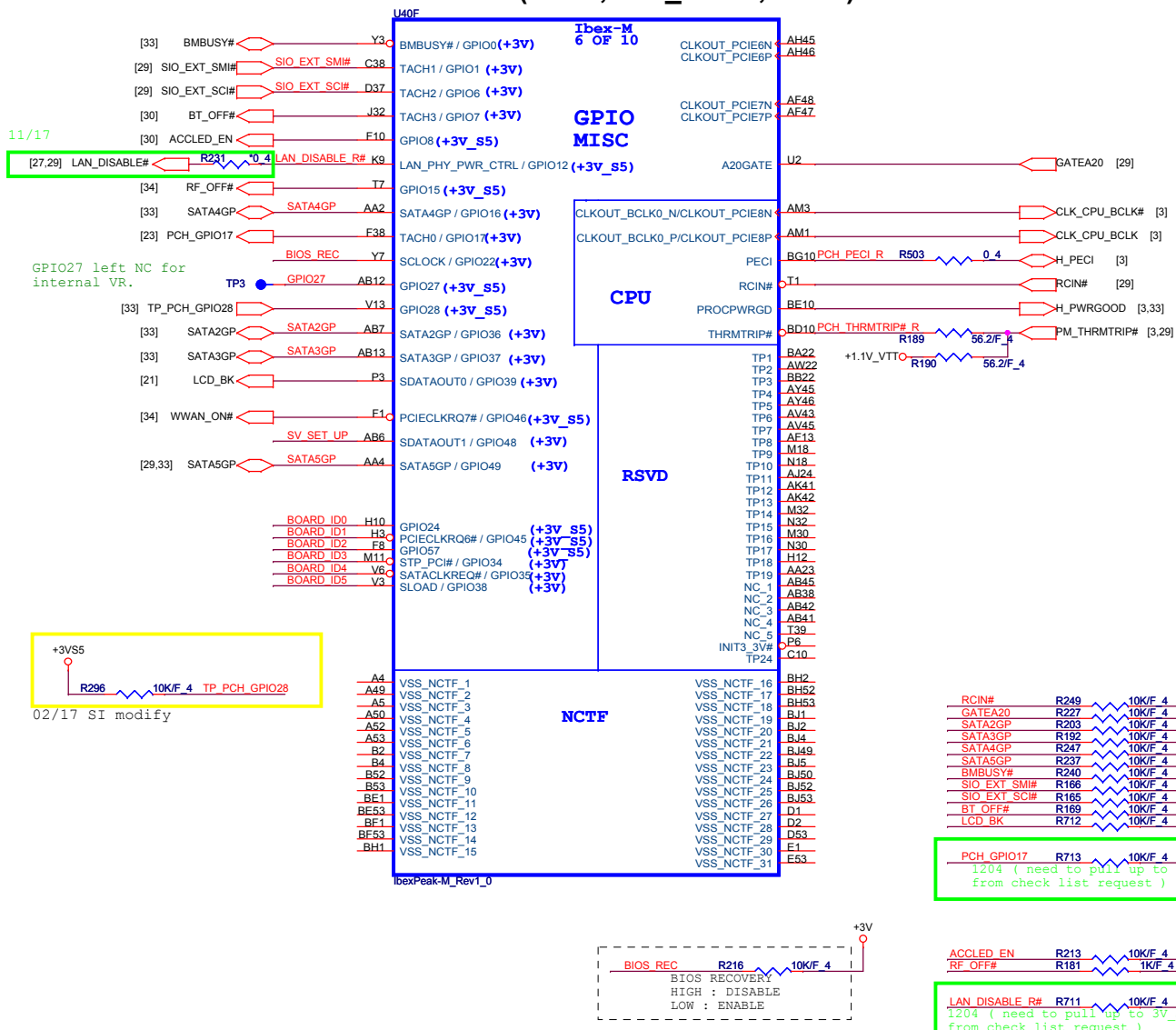
[2,7,8,11,14,15,16,28,29,33,36] +1.05V
[2,3,7,8,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[8,10,11,31,33,40] +3VS5

NB5

PROJECT : UP67
Quanta Computer Inc.

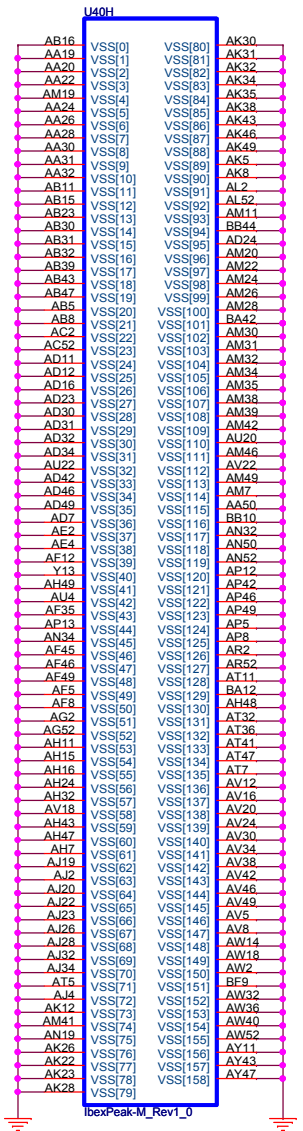
Size	Document Number	Rev
Custom	PCH 6/6 (GND)/ Braidwood	1A
Date: Monday, October 26, 2009	Sheet 9 of 45	

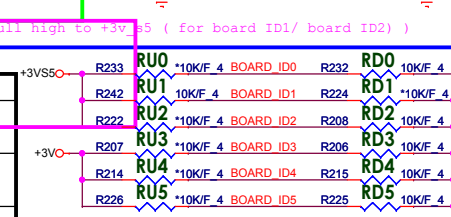
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



SI 0305(PCH GPIO 45 / GPIO50 pull high to +3V_S5 (for board ID1/ board ID2))

IBEX PEAK-M (GND)





BOARD ID SETTING

Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UP6/7	0=UP6 1=UP7					
UMA/Dis.		0=UMA 1=Dis.				
Project name			00=Jones/Cujo 2.0 (Clarksfield) 10=Jones/Cujo 2.1 (Auburndale UMA)			
ROM Size					0= 2M 1= 4M	

[2,3,7,8,9,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[8,9,11,31,33,40] +3VS5
[3,5,11,33,37,38] +1.1V_VTT
[5,11,33,36,40] +1.8V

10

[9] GNT3# R472 *10K_NC

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP R223 10K/F_4 +3V

SV_SET_UP	1-X High = Strong (Default)

[9] GNT0#
[9] GNT1#
GNT0# R150 *1K/F_4
GNT1# R471 *1K/F_4
BIOS boot from SPI
SI 2/5 modified

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

[9,33] NV_ALE R505 *1K/F_4
[9,33] NV_CLE R506 *1K/F_4
11/17
+1.8V

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap

[7,24,25] SPKR SPKR *1K/F_4 R313 +3V
[7] PCH_GPIO33 R170 *100K/F_4
SI 2/5 modified

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO & Strap)	1A
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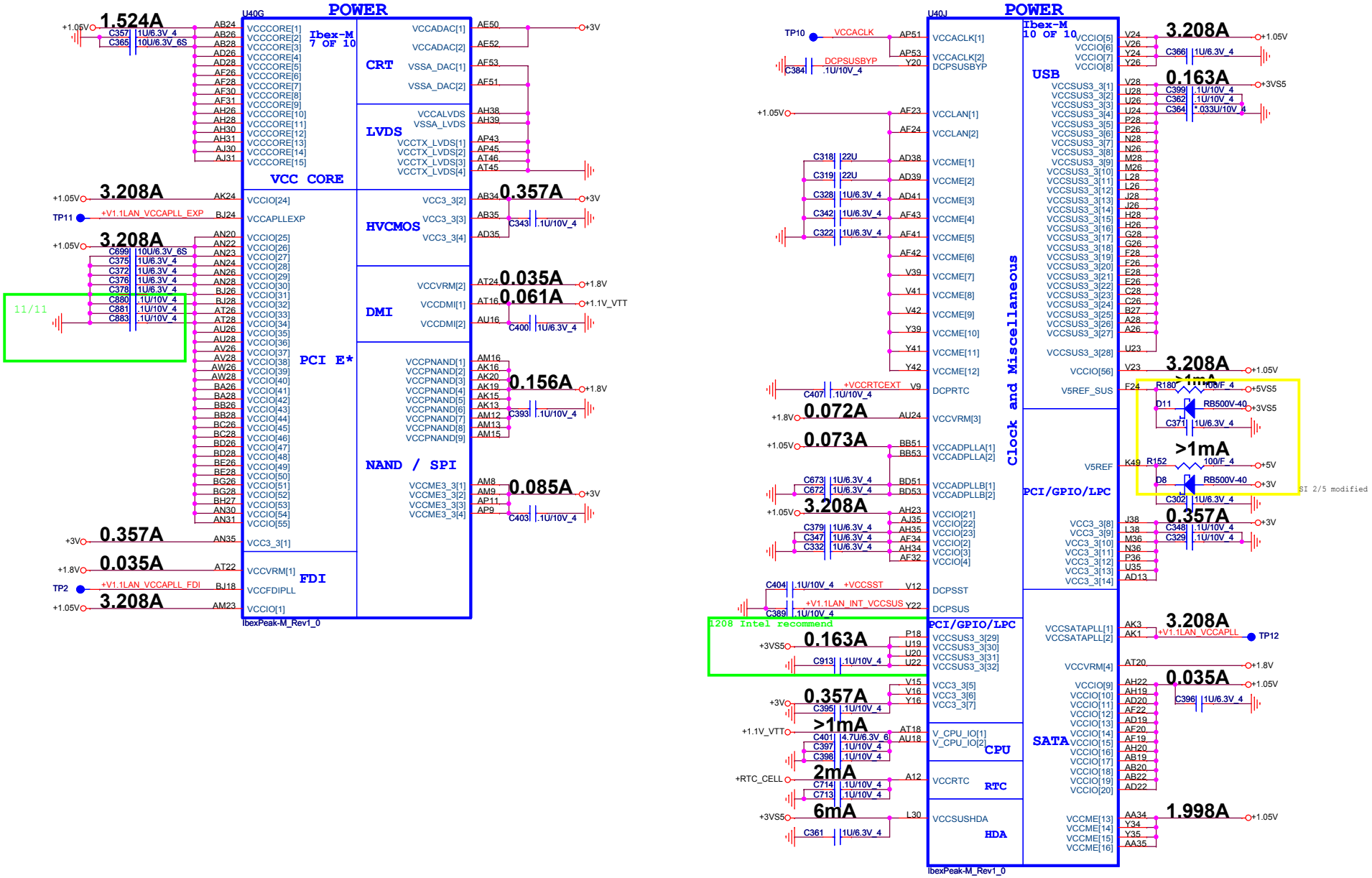
NB5



[2,7,8,9,14,15,16,28,29,33,36] +1.05V
[3,5,10,33,37,38] +1.1V_VTT
[5,10,33,36,40] +1.8V
[2,3,7,8,9,10,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[8,9,10,31,33,40] +3VS5
[21,22,24,25,30,31,32,34,40] +5V
[40] +5VS5

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A

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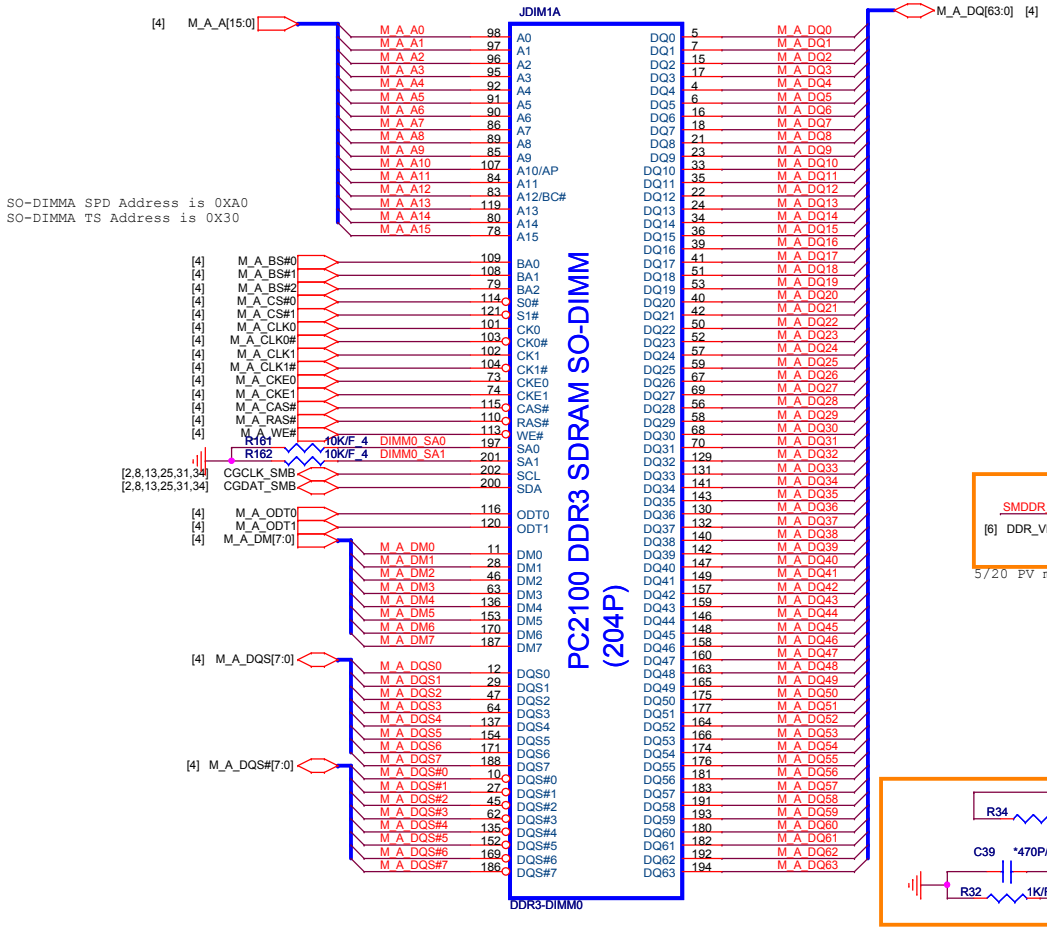
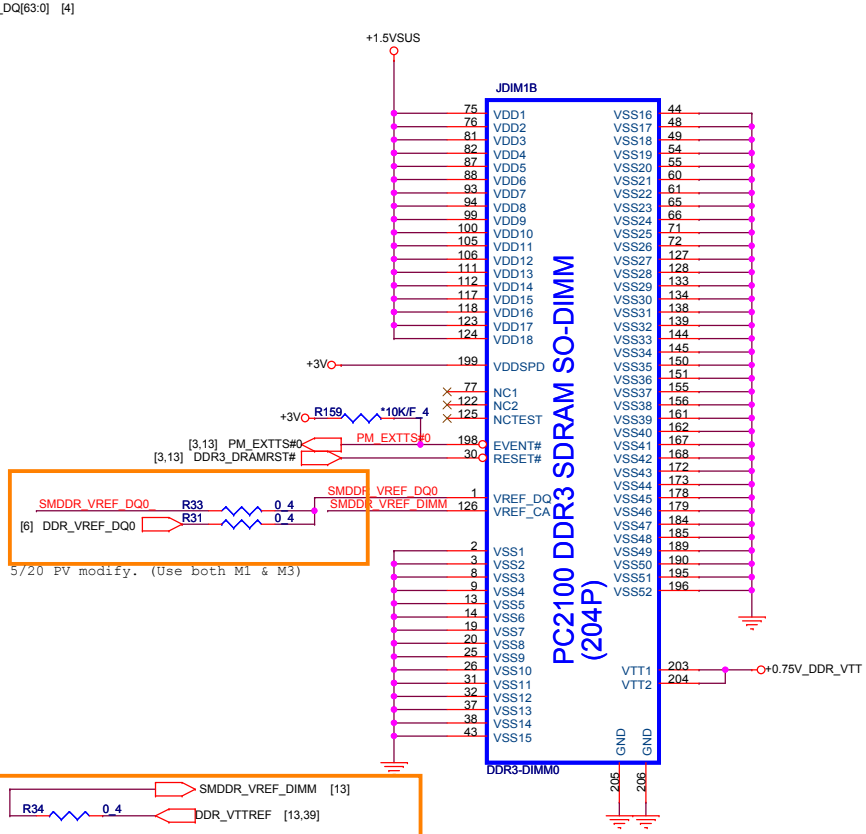
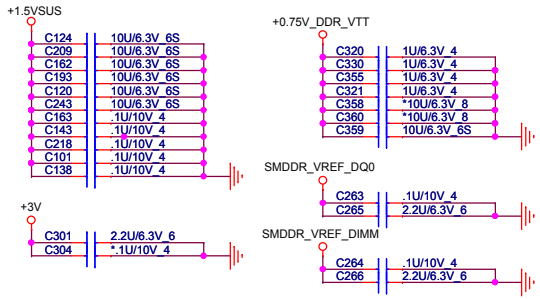




Place these Caps near So-Dimm0.

11/6



5/20: NA for INT recommand

reserve only..
can let it NC at this block components if DB stage not trouble found

[13,39] +0.75V_DDR_VTT
[3,5,13,39] +1.5VSUS
[2,3,7,8,9,10,11,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,13,21,29,30,31,32,34,35,36,38,40,41] +3VPCU
[24,25,29,31,35,36,37,38,39,40] +5VPCU

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A

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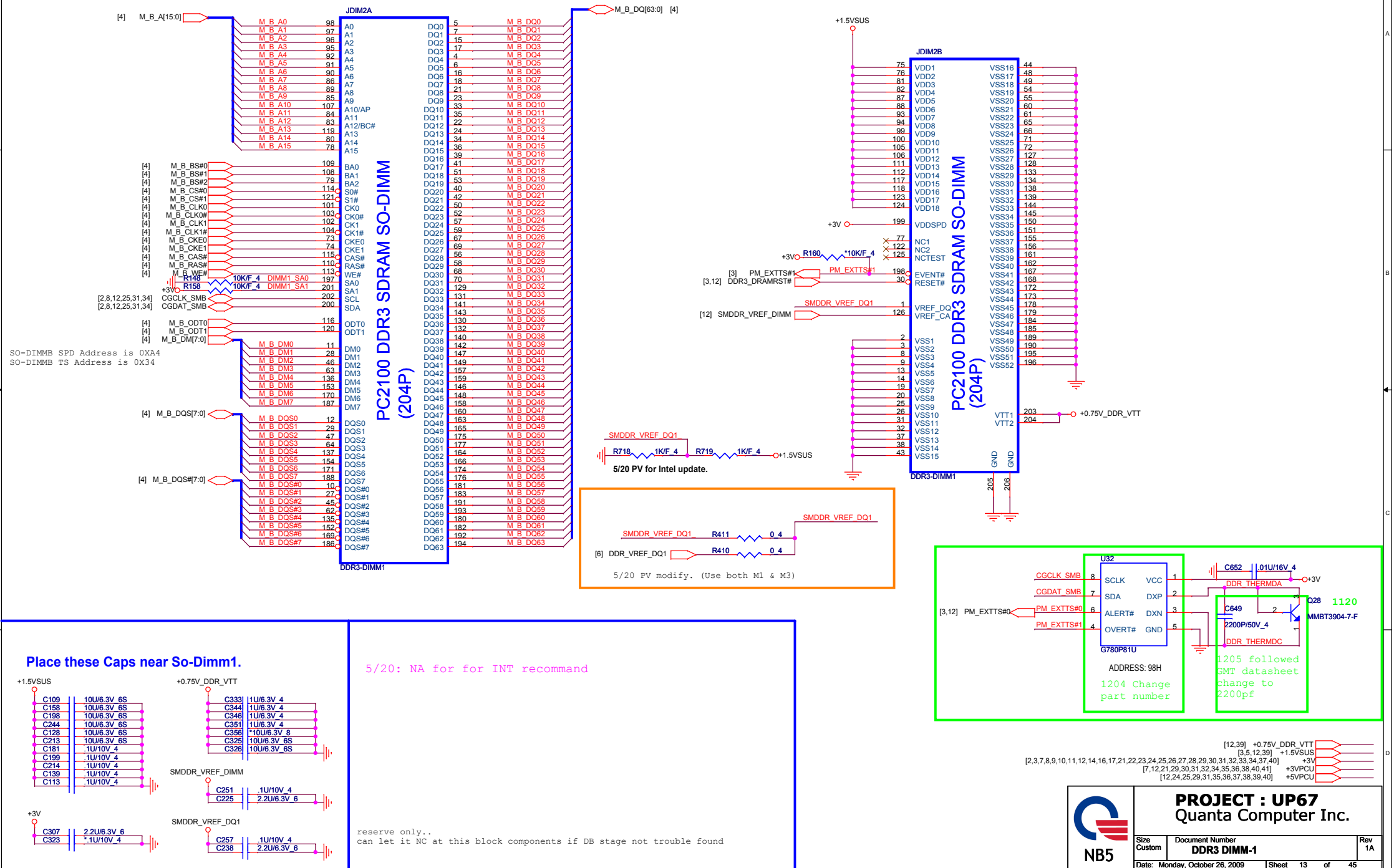

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Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: DDR3 DIMM-1
Rev: 1A	
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PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

~ 500mA

1600mA

Near BGA

12~16 mils width
110mA

PCI EXPRESS

SI 2/13 modified

11/12

11/10 for placement

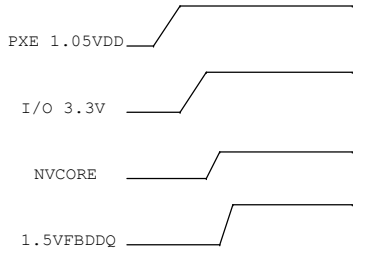
SI 2/13 modified

L211 for Nvidia request
add transition cap

VGA Thermal Circuit

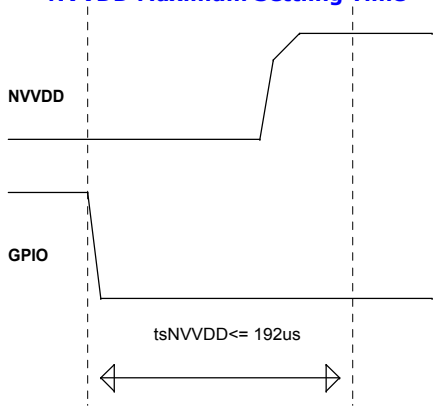
0514: PV modify
Delete Reserved thermal circuit

power up sequence

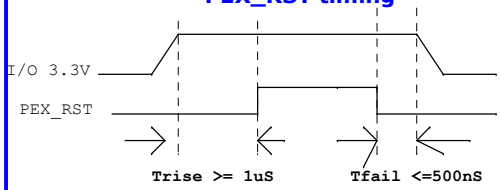


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing



[2,7,8,9,11,15,16,28,29,33,36] +1.05V
[2,3,7,8,9,10,11,12,13,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V

NB5	PROJECT : UP67 Quanta Computer Inc.	
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U35B

BGA969-NVIDIA-NB9P-GS
COMMON

12/02 modify
package for N10

MEMORY I/F A

U35C

BGA969-NVIDIA-NB9P-GS
COMMON

12/02 modify
package for N10

MEMORY I/F C

Memory clk spread : down 1.25% (30~33KHz)

use internal Vref, ext divider no stuff

15mils width

For Debug only

SI 2/13 modified

SI 2/5 Modified

12/16 Modified

R92 no stuff

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Quanta Computer Inc.	
Size: Custom	Document Number: N10X (MEMORY I/F) 2/5
Rev: 1A	
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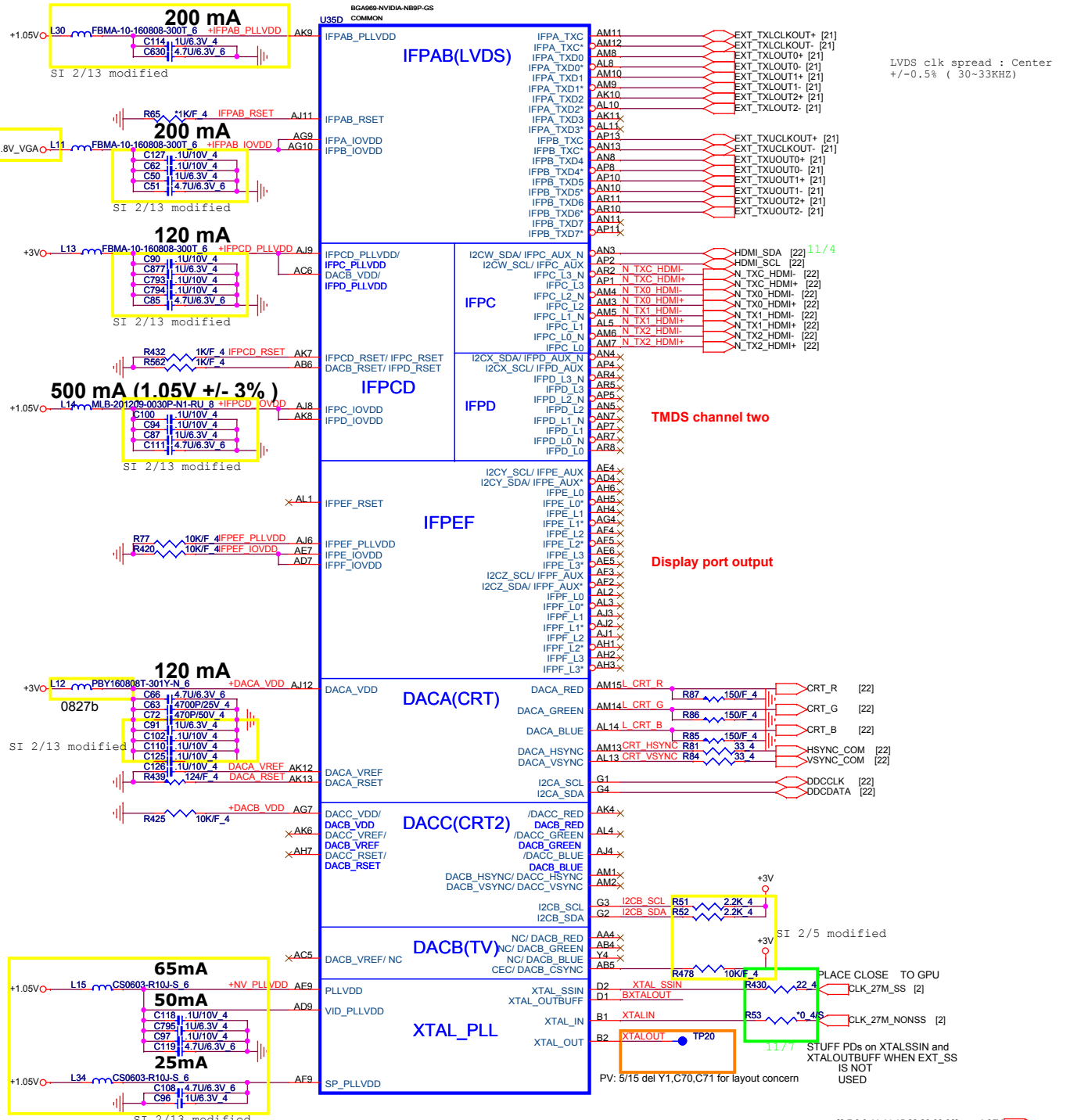
NB5



PROJECT	UP67 Quanta Computer Inc.
Size / Document Number	Custom / N10X (DISPLAY) 3/5
Rev	2A
Date	Monday, October 26, 2009
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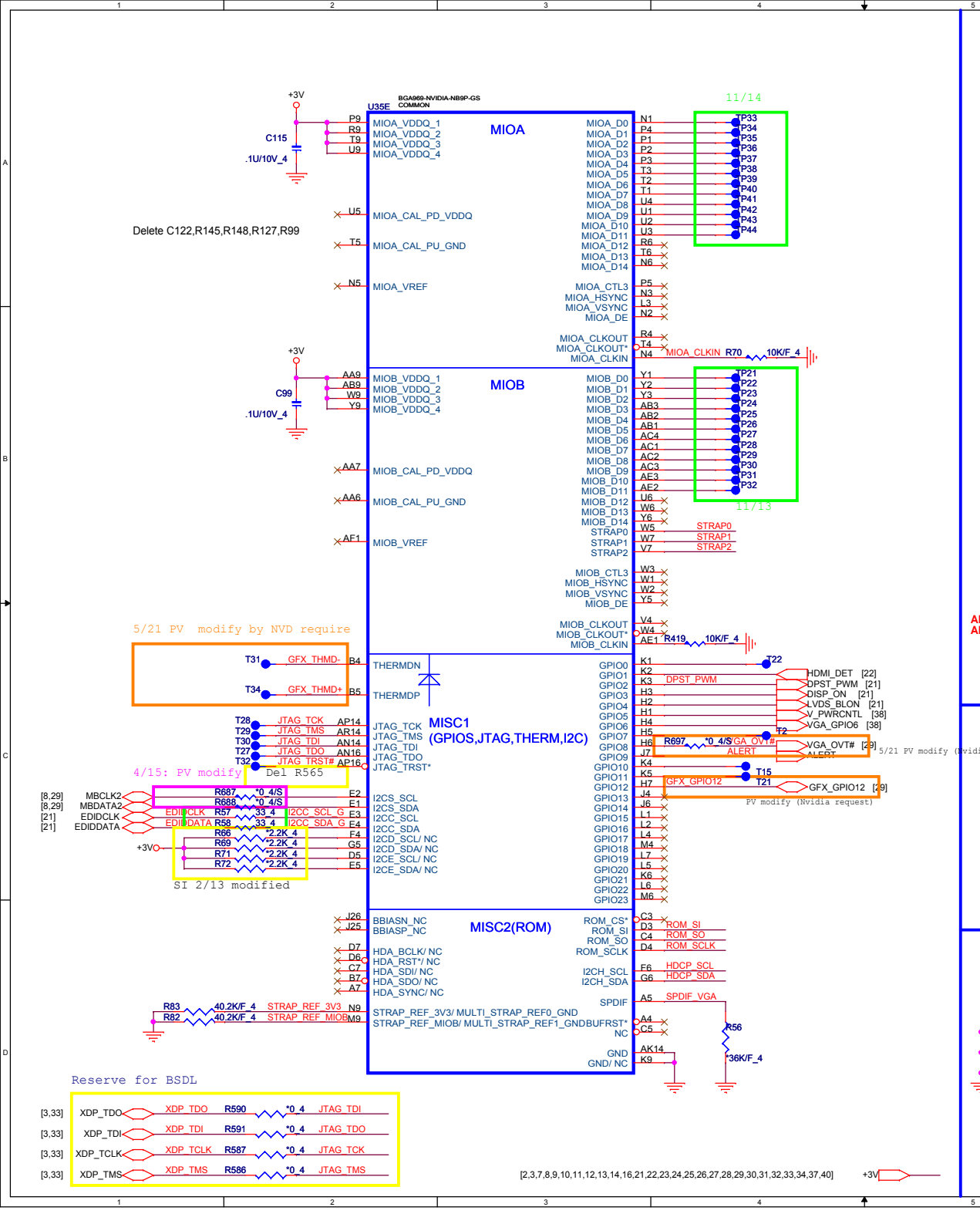
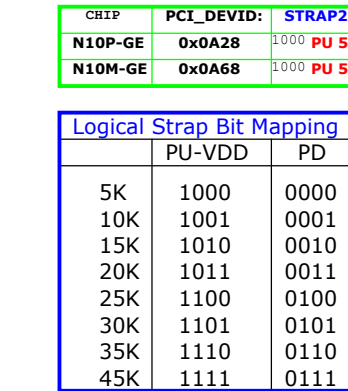
NB5	





DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

CHIP	PCI_DEVID:	STRAP2
N10P-GE	0x0A28	1000 PU 5K
N10M-GE	0x0A68	1000 PU 5K

SEE Datasheet for details on N10P Straps!

17

PCI_DEVID[4]/SUBVENDOR

1211 DEVICE ID CHANGE

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

(Ra)

Default: Hynix VRAM

CS31002FB26 (RES CHIP 10K 1/16W +-1% (0402))
CS31502FB08 (RES CHIP 15K 1/16W +-1% (0402))
CS32002FB02 (RES CHIP 20K 1/16W +-1%(0402))

PV modify 6/1 (NV require)
change R63 to 34.8 kohm.R62
NA.

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

(Ra)

	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
	0000		Reserved		
AKD58GGT^01	0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
AKD5LZGTW00	0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
	0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
	0101		Reserved		
	0110				
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10X (GPIO & STRAPS) 4/5	2A
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U35F

BGA969-NVIDIA-NB9P-GS
COMMON

+VGACORE

+VGACORE

NVVDD

AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T16
AC24	VDD_022	VDD_078	T18
AC25	VDD_023	VDD_079	T20
AD12	VDD_024	VDD_080	T22
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V17
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

02/16 SI modify

NVVDD Decoupling

PLACE NEAR BALLS

+VGACORE

C74	*4.7U/6.3V_6
C155	1U/6.3V_4
C73	.22U/25V_6
C135	.22U/25V_6
C134	1U/10V_4
C215	.022U/16V_4
C201	.022U/16V_4
C140	.022U/16V_4
C164	.022U/16V_4
C200	.047U/16V_4
C182	.047U/16V_4
C216	.047U/16V_4
C169	.01U/16V_4
C183	.01U/16V_4
C184	.01U/16V_4
C217	.01U/16V_4
C132	.01U/16V_4
C185	.01U/16V_4
C203 2 1	4700P/25V_4
C202 2 1	4700P/25V_4
C78	330U/2.5V_6032

U35G

BGA969-NVIDIA-NB9P-GS
COMMON

GROUND

AA11	GND_1	GND_096	E15
AA12	GND_2	GND_097	E18
AA13	GND_3	GND_098	E24
AA14	GND_4	GND_099	E27
AA15	GND_5	GND_100	E30
AA16	GND_6	GND_101	E6
AA17	GND_7	GND_102	E9
AA18	GND_8	GND_103	F2
AA19	GND_9	GND_104	F31
AA2	GND_10	GND_105	F34
AA20	GND_11	GND_106	F5
AA21	GND_12	GND_107	J2
AA22	GND_13	GND_108	J31
AA23	GND_14	GND_109	J34
AA24	GND_15	GND_110	J5
AA25	GND_16	GND_111	L9
AA34	GND_17	GND_112	M11
AA5	GND_18	GND_113	M13
AB12	GND_19	GND_114	M15
AB14	GND_20	GND_115	M17
AB16	GND_21	GND_116	M19
AB18	GND_22	GND_117	M2
AB20	GND_23	GND_118	M21
AB22	GND_24	GND_119	M23
AB24	GND_25	GND_120	M25
AC9	GND_26	GND_121	M31
AD11	GND_27	GND_122	M34
AD13	GND_28	GND_123	M5
AD15	GND_29	GND_124	N11
AD17	GND_30	GND_125	N12
AD2	GND_31	GND_126	N13
AD21	GND_32	GND_127	N14
AD23	GND_33	GND_128	N15
AD25	GND_34	GND_129	N16
AD31	GND_35	GND_130	N17
AD34	GND_36	GND_131	N18
AD5	GND_37	GND_132	N19
AE11	GND_38	GND_133	N20
AE12	GND_39	GND_134	N21
AE13	GND_40	GND_135	N22
AE14	GND_41	GND_136	N23
AE15	GND_42	GND_137	N24
AE16	GND_43	GND_138	N25
AE17	GND_44	GND_139	P12
AE18	GND_45	GND_140	P14
AE19	GND_46	GND_141	P16
AE20	GND_47	GND_142	P18
AE21	GND_48	GND_143	P20
AE22	GND_49	GND_144	P22
AE23	GND_50	GND_145	P24
AE24	GND_51	GND_146	R2
AE25	GND_52	GND_147	R31
AG2	GND_53	GND_148	R34
AG31	GND_54	GND_149	R5
AG34	GND_55	GND_150	T11
AG5	GND_56	GND_151	T13
AK2	GND_57	GND_152	T15
AK31	GND_58	GND_153	T17
AK34	GND_59	GND_154	T19
AK5	GND_60	GND_155	T21
AL12	GND_61	GND_156	T23
AL15	GND_62	GND_157	T25
AL18	GND_63	GND_158	U11
AL21	GND_64	GND_159	U12
AL24	GND_65	GND_160	U13
AL27	GND_66	GND_161	U14
AL30	GND_67	GND_162	U15
AL6	GND_68	GND_163	U16
AL9	GND_69	GND_164	U17
AN2	GND_70	GND_165	U18
AN34	GND_71	GND_166	U19
AP12	GND_72	GND_167	U20
AP15	GND_73	GND_168	U21
AP18	GND_74	GND_169	U22
AP21	GND_75	GND_170	U23
AP24	GND_76	GND_171	U24
AP27	GND_77	GND_172	U25
AP3	GND_78	GND_173	V12
AP30	GND_79	GND_174	V14
AP33	GND_80	GND_175	V16
AP6	GND_081	GND_176	V18
AP9	GND_082	GND_177	V2
B12	GND_083	GND_178	V20
B15	GND_084	GND_179	V22
B21	GND_085	GND_180	V24
B24	GND_086	GND_181	V31
B27	GND_087	GND_182	V5
B3	GND_088	GND_183	V9
B30	GND_089	GND_184	Y11
B33	GND_090	GND_185	Y13
B6	GND_091	GND_186	Y15
B9	GND_092	GND_187	Y17
C2	GND_093	GND_188	Y19
C34	GND_094	GND_189	Y21
E12	GND_095	GND_190	Y23
		GND_191	Y25

Del all VRAM termination
(RP16~RP75)

SI 2/5 modified

[38] +VGACORE
[15,19,20,31,34,36,39,40] +1.5V

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10X (POWER & GND) 5/5	2A

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CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

U46 / U47 / U48 / U49 — VRAM_DDR3 — 96-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R572 243/F_4 (U46)
R573 243/F_4 (U47)
R574 243/F_4 (U48)
R575 243/F_4 (U49)

11/12 VMA_WDQS2 / VMA_RDQS2 DQSL DQSL
11/12 VMA_WDQS0 / VMA_RDQS0 DQSU DQSU
11/12 VMA_WDQS3 / VMA_RDQS3 DQSL DQSL
11/12 VMA_WDQS1 / VMA_RDQS1 DQSU DQSU
11/17 Swap VMA_WDQS5 / VMA_RDQS5 DQSL DQSL
11/17 Swap VMA_WDQS4 / VMA_RDQS4 DQSU DQSU
VMA_WDQS7 / VMA_RDQS7 DQSL DQSL
VMA_WDQS6 / VMA_RDQS6 DQSU DQSU

02/16 SI modify
R592 121/F_4 VMA_CLK0
VMA_CLK0_COMM C806 *.01U/16V_4
R594 121/F_4 VMA_CLK0#

11/11 +1.5V
R576 1.33K/F_4 VREFC_VMA1
R584 1.33K/F_4 C798 .1U/10V_4
11/11 +1.5V
R577 1.33K/F_4 VREFD_VMA1
R585 1.33K/F_4 C799 .1U/10V_4

02/16 SI modify
R593 121/F_4 VMA_CLK1
VMA_CLK1_COMM C823 *.01U/16V_4
R595 121/F_4 VMA_CLK1#

11/11 +1.5V
R580 1.33K/F_4 VREFC_VMA3
R588 1.33K/F_4 C802 .1U/10V_4
11/11 +1.5V
R581 1.33K/F_4 VREFD_VMA3
R589 1.33K/F_4 C803 .1U/10V_4

+1.5V
C825 C826 C829 C830 1U/6.3V_4
+1.5V
C818 10U/6.3V_6S
C827 C831 C833 C832 C828 .1U/10V_4
+1.5V
C807 C808 C809 C810 C811 C812 C813 C814 .1U/10V_4
+1.5V
C815 C816 C817 C824 C819 C820 C821 C822 .1U/10V_4
+1.5V
C914 C915 C916 C917 .1U/10V_4

1211 for Nvidia request add transition cap

[15,20,31,34,36,39,40] +1.5V

PROJECT : UP67
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	VRAM channel A	1A
Date: Monday, October 26, 2009	Sheet 19 of 45	

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

CHANNEL B: 256MB/512MB DDR3

U50 — VRAM _DDR3 — 96-BALL SDRAM DDR3

VREFC_VMC1 M8 — VREFCA
VREFD_VMC1 H1 — VREFDQ

[15] FBC_CMD19 N3 — A0
[15] FBC_CMD25 P7 — A1
[15] FBC_CMD22 P3 — A2
[15] FBC_CMD24 N2 — A3
[15] FBC_CMD0 P8 — A4
[15] FBC_CMD2 P2 — A5
[15] FBC_CMD21 R8 — A6
[15] FBC_CMD16 R2 — A7
[15] FBC_CMD23 T8 — A8
[15] FBC_CMD20 R3 — A9
[15] FBC_CMD17 L7 — A10/AP
[15] FBC_CMD9 R7 — A11
[15] FBC_CMD14 N7 — A12/BC
[15] FBC_CMD26 T3 — A13
T7 — A14
M7 — A15

[15] FBC_CMD12 M2 — BA0
[15] FBC_CMD3 N8 — BA1
[15] FBC_CMD27 M3 — BA2

[15] VMC_CLK0 J7 — CK
[15] VMC_CLK0# K7 — CK
[15] FBC_CMD18 K9 — CKE

[15] FBC_CMD30 K1 — ODT
[15] FBC_CMD29 L2 — CS
[15] FBC_CMD1 J3 — RAS
[15] FBC_CMD10 K3 — CAS
[15] FBC_CMD11 L3 — WE

VMC_WDQS2 F3 — DQSL
VMC_RDQS2 G3 — DQSL

VMC_DM2 E7 — DML
VMC_DM0 D3 — DMU

VMC_WDQS0 C7 — DQSU
VMC_RDQS0 B7 — DQSU

[15] FBC_CMD15 T2 — RESET

VMC_ZQ1 L8 — ZQ

R596 243/F_4

J1 — NC#J1
L1 — NC#L1
J9 — NC#J9
L9 — NC#L9

DQL0 E3 — VMC_DQ22
DQL1 F7 — VMC_DQ21
DQL2 F2 — VMC_DQ23
DQL3 F8 — VMC_DQ16
DQL4 H3 — VMC_DQ20
DQL5 H8 — VMC_DQ17
DQL6 G2 — VMC_DQ18
DQL7 H7 — VMC_DQ19

DQU0 D7 — VMC_DQ2
DQU1 C3 — VMC_DQ4
DQU2 C8 — VMC_DQ0
DQU3 C2 — VMC_DQ6
DQU4 A7 — VMC_DQ1
DQU5 A2 — VMC_DQ7
DQU6 B8 — VMC_DQ3
DQU7 A3 — VMC_DQ5

VDD#B2 B2 — +1.5V
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9 — +1.5V

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

Should be 240 Ohms +-1%

11/11
R617 121/F_4 — VMC_CLK0
VMC_CLK0_COMM — C859 .01U/16V_4
R619 121/F_4 — VMC_CLK0#

U51 — VRAM _DDR3 — 96-BALL SDRAM DDR3

VREFC_VMC1 M8 — VREFCA
VREFD_VMC1 H1 — VREFDQ

FBC_CMD19 N3 — A0
FBC_CMD25 P7 — A1
FBC_CMD22 P3 — A2
FBC_CMD24 N2 — A3
FBC_CMD0 P8 — A4
FBC_CMD2 P2 — A5
FBC_CMD21 R8 — A6
FBC_CMD16 R2 — A7
FBC_CMD23 T8 — A8
FBC_CMD20 R3 — A9
FBC_CMD17 L7 — A10/AP
FBC_CMD9 R7 — A11
FBC_CMD14 N7 — A12/BC
FBC_CMD26 T3 — A13
T7 — A14
M7 — A15

FBC_CMD12 M2 — BA0
FBC_CMD3 N8 — BA1
FBC_CMD27 M3 — BA2

VMC_CLK0 J7 — CK
VMC_CLK0# K7 — CK
FBC_CMD18 K9 — CKE

FBC_CMD30 K1 — ODT
FBC_CMD29 L2 — CS
FBC_CMD1 J3 — RAS
FBC_CMD10 K3 — CAS
FBC_CMD11 L3 — WE

11/12
VMC_WDQS3 F3 — DQSL
VMC_RDQS3 G3 — DQSL

VMC_DM3 E7 — DML
VMC_DM1 D3 — DMU

11/12
VMC_WDQS1 C7 — DQSU
VMC_RDQS1 B7 — DQSU

FBC_CMD15 T2 — RESET

VMC_ZQ2 L8 — ZQ

R597 243/F_4

J1 — NC#J1
L1 — NC#L1
J9 — NC#J9
L9 — NC#L9

DQL0 E3 — VMC_DQ28
DQL1 F7 — VMC_DQ24
DQL2 F2 — VMC_DQ31
DQL3 F8 — VMC_DQ27
DQL4 H3 — VMC_DQ30
DQL5 H8 — VMC_DQ25
DQL6 G2 — VMC_DQ29
DQL7 H7 — VMC_DQ26

DQU0 D7 — VMC_DQ8
DQU1 C3 — VMC_DQ14
DQU2 C8 — VMC_DQ9
DQU3 C2 — VMC_DQ12
DQU4 A7 — VMC_DQ11
DQU5 A2 — VMC_DQ13
DQU6 B8 — VMC_DQ10
DQU7 A3 — VMC_DQ15

VDD#B2 B2 — +1.5V
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9 — +1.5V

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

Should be 240 Ohms +-1%

11/11
+1.5V
R600 1.33K/F_4 — VREFC_VMC1
R608 1.33K/F_4 — C834 .1U/10V_4

11/11
+1.5V
R601 1.33K/F_4 — VREFD_VMC1
R609 1.33K/F_4 — C835 .1U/10V_4

U52 — VRAM _DDR3 — 96-BALL SDRAM DDR3

VREFC_VMC3 M8 — VREFCA
VREFD_VMC3 H1 — VREFDQ

[15] FBC_CMD4 P3 — A1
[15] FBC_CMD6 N2 — A3
[15] FBC_CMD5 P8 — A4
[15] FBC_CMD13 P2 — A5

FBC_CMD19 N3 — A0
FBC_CMD25 P7 — A1
FBC_CMD4 P3 — A2
FBC_CMD6 N2 — A3
FBC_CMD5 P8 — A4
FBC_CMD13 P2 — A5
FBC_CMD21 R8 — A6
FBC_CMD16 R2 — A7
FBC_CMD23 T8 — A8
FBC_CMD20 R3 — A9
FBC_CMD17 L7 — A10/AP
FBC_CMD9 R7 — A11
FBC_CMD14 N7 — A12/BC
FBC_CMD26 T3 — A13
T7 — A14
M7 — A15

FBC_CMD12 M2 — BA0
FBC_CMD3 N8 — BA1
FBC_CMD27 M3 — BA2

[15] VMC_CLK1 J7 — CK
[15] VMC_CLK1# K7 — CK
[15] FBC_CMD7 K9 — CKE

[15] FBC_CMD28 K1 — ODT
[15] FBC_CMD8 L2 — CS
FBC_CMD1 J3 — RAS
FBC_CMD10 K3 — CAS
FBC_CMD11 L3 — WE

11/12
VMC_WDQS4 F3 — DQSL
VMC_RDQS4 G3 — DQSL

VMC_DM4 E7 — DML
VMC_DM5 D3 — DMU

11/12
VMC_WDQS5 C7 — DQSU
VMC_RDQS5 B7 — DQSU

FBC_CMD15 T2 — RESET

VMC_ZQ3 L8 — ZQ

R598 243/F_4

J1 — NC#J1
L1 — NC#L1
J9 — NC#J9
L9 — NC#L9

DQL0 E3 — VMC_DQ34
DQL1 F7 — VMC_DQ36
DQL2 F2 — VMC_DQ32
DQL3 F8 — VMC_DQ39
DQL4 H3 — VMC_DQ33
DQL5 H8 — VMC_DQ38
DQL6 G2 — VMC_DQ35
DQL7 H7 — VMC_DQ37

DQU0 D7 — VMC_DQ41
DQU1 C3 — VMC_DQ47
DQU2 C8 — VMC_DQ40
DQU3 C2 — VMC_DQ45
DQU4 A7 — VMC_DQ44
DQU5 A2 — VMC_DQ43
DQU6 B8 — VMC_DQ42
DQU7 A3 — VMC_DQ46

VDD#B2 B2 — +1.5V
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9 — +1.5V

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

Should be 240 Ohms +-1%

11/11
R616 121/F_4 — VMC_CLK1
VMC_CLK1_COMM — C858 .01U/16V_4
R618 121/F_4 — VMC_CLK1#

U53 — VRAM _DDR3 — 96-BALL SDRAM DDR3

VREFC_VMC3 M8 — VREFCA
VREFD_VMC3 H1 — VREFDQ

FBC_CMD19 N3 — A0
FBC_CMD25 P7 — A1
FBC_CMD4 P3 — A2
FBC_CMD6 N2 — A3
FBC_CMD5 P8 — A4
FBC_CMD13 P2 — A5
FBC_CMD21 R8 — A6
FBC_CMD16 R2 — A7
FBC_CMD23 T8 — A8
FBC_CMD20 R3 — A9
FBC_CMD17 L7 — A10/AP
FBC_CMD9 R7 — A11
FBC_CMD14 N7 — A12/BC
FBC_CMD26 T3 — A13
T7 — A14
M7 — A15

FBC_CMD12 M2 — BA0
FBC_CMD3 N8 — BA1
FBC_CMD27 M3 — BA2

VMC_CLK1 J7 — CK
VMC_CLK1# K7 — CK
FBC_CMD7 K9 — CKE

FBC_CMD28 K1 — ODT
FBC_CMD8 L2 — CS
FBC_CMD1 J3 — RAS
FBC_CMD10 K3 — CAS
FBC_CMD11 L3 — WE

11/12
VMC_WDQS6 F3 — DQSL
VMC_RDQS6 G3 — DQSL

VMC_DM6 E7 — DML
VMC_DM7 D3 — DMU

11/12
VMC_WDQS7 C7 — DQSU
VMC_RDQS7 B7 — DQSU

FBC_CMD15 T2 — RESET

VMC_ZQ4 L8 — ZQ

R599 243/F_4

J1 — NC#J1
L1 — NC#L1
J9 — NC#J9
L9 — NC#L9

DQL0 E3 — VMC_DQ49
DQL1 F7 — VMC_DQ48
DQL2 F2 — VMC_DQ55
DQL3 F8 — VMC_DQ53
DQL4 H3 — VMC_DQ52
DQL5 H8 — VMC_DQ50
DQL6 G2 — VMC_DQ54
DQL7 H7 — VMC_DQ51

DQU0 D7 — VMC_DQ61
DQU1 C3 — VMC_DQ57
DQU2 C8 — VMC_DQ62
DQU3 C2 — VMC_DQ59
DQU4 A7 — VMC_DQ60
DQU5 A2 — VMC_DQ56
DQU6 B8 — VMC_DQ63
DQU7 A3 — VMC_DQ58

VDD#B2 B2 — +1.5V
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9 — +1.5V

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

Should be 240 Ohms +-1%

11/11
+1.5V
R604 1.33K/F_4 — VREFC_VMC3
R612 1.33K/F_4 — C838 .1U/10V_4

11/11
+1.5V
R605 1.33K/F_4 — VREFD_VMC3
R613 1.33K/F_4 — C839 .1U/10V_4

+1.5V
C865 1U/6.3V_4
C866 1U/6.3V_4
C844 1U/6.3V_4
C855 1U/6.3V_4

+1.5V
C863 10U/6.3V_6S
C862 .1U/10V_4
C867 .1U/10V_4
C868 .1U/10V_4
C869 .1U/10V_4
C864 .1U/10V_4

+1.5V
C842 .1U/10V_4
C843 .1U/10V_4
C860 .1U/10V_4
C845 .1U/10V_4
C846 .1U/10V_4
C847 .1U/10V_4
C848 .1U/10V_4
C849 .1U/10V_4

+1.5V
C850 .1U/10V_4
C851 .1U/10V_4
C852 .1U/10V_4
C853 .1U/10V_4
C854 .1U/10V_4
C861 .1U/10V_4
C856 .1U/10V_4
C857 .1U/10V_4

[15,19,31,34,36,39,40] +1.5V

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM channel B	1A

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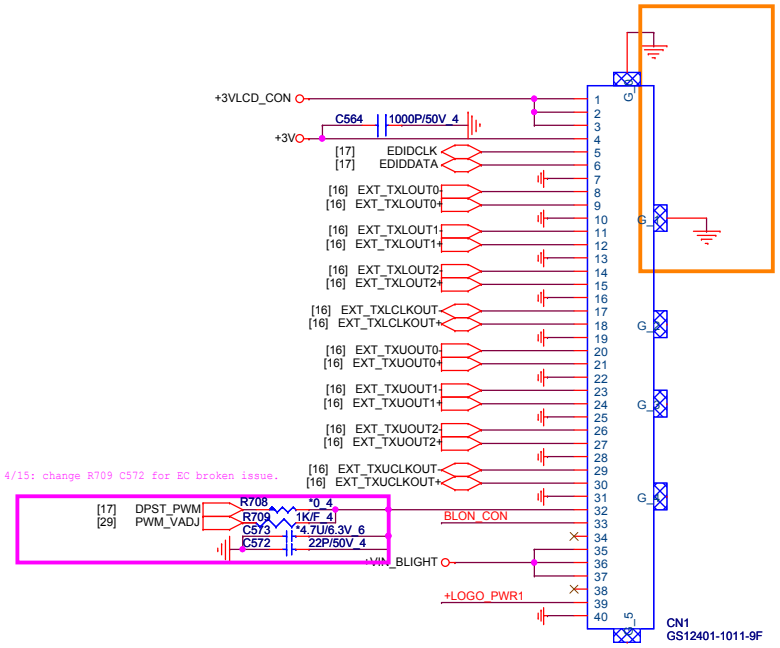
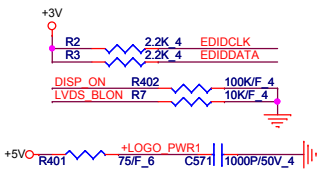
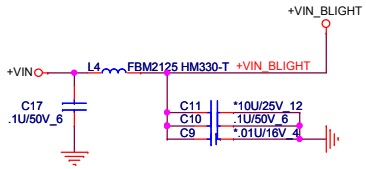
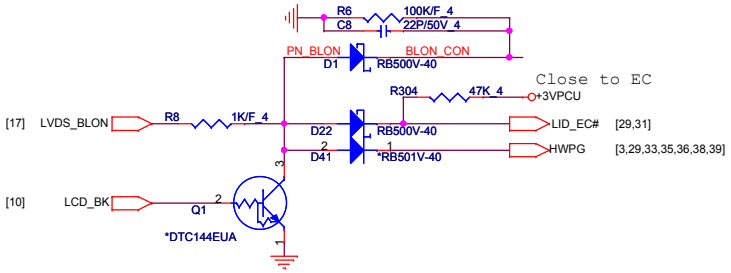
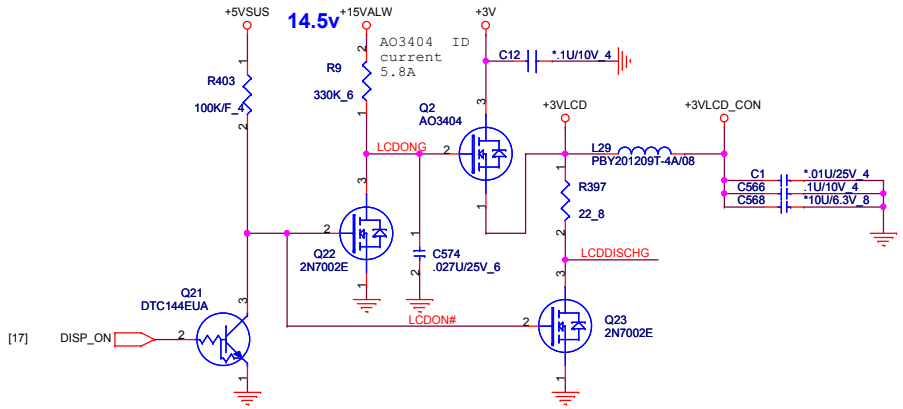
5/20: change PIN 41,PIN42 to GND pad for EMI.











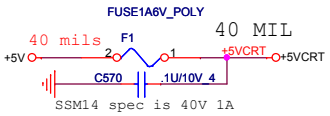
[2,3,7,8,9,10,11,12,13,14,16,17,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,12,13,29,30,31,32,34,35,36,38,40,41] +3VPCU
[11,22,24,25,30,31,32,34,40] +5V
[30,32,40] +5VSUS
[31,35,40] +15VALW
[26,32,35,36,37,38,39,40,41] +VIN

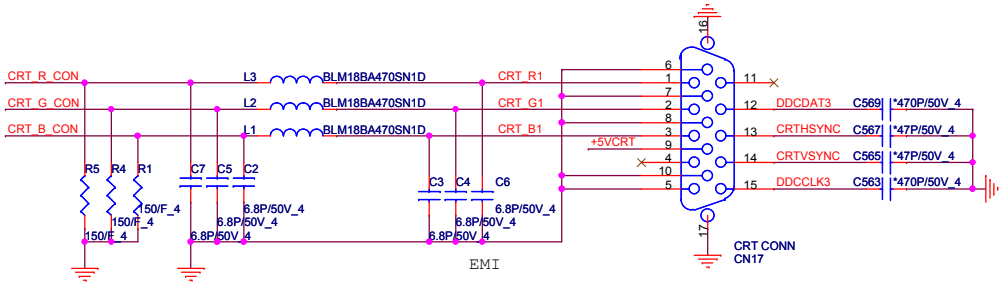
NB5

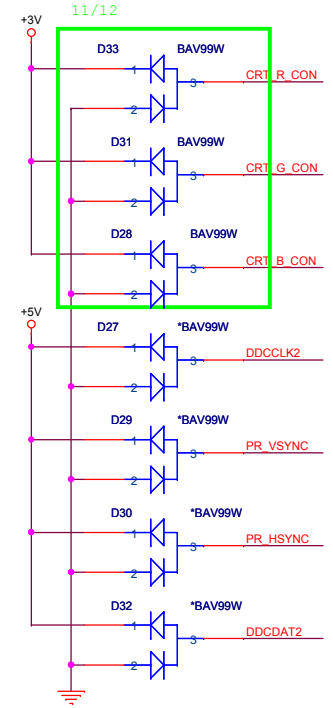
PROJECT : UP67
Quanta Computer Inc.

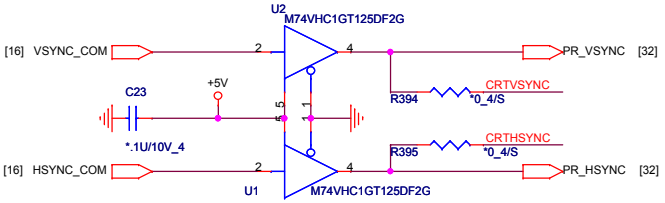
Size	Document Number	Rev
Custom	LCD CONN/LID function	1A
Date: Monday, October 26, 2009	Sheet 21 of 45	

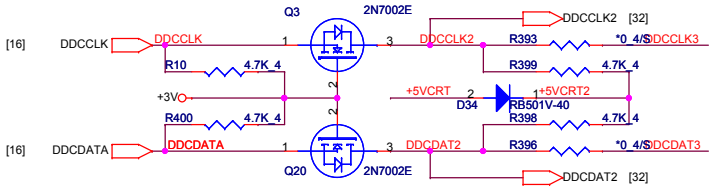
CRT PORT



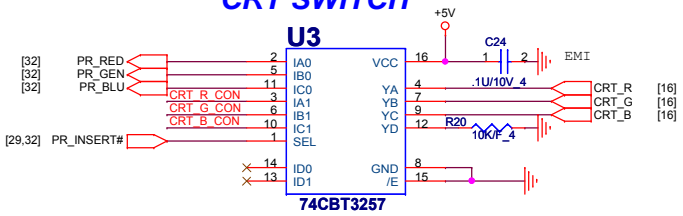






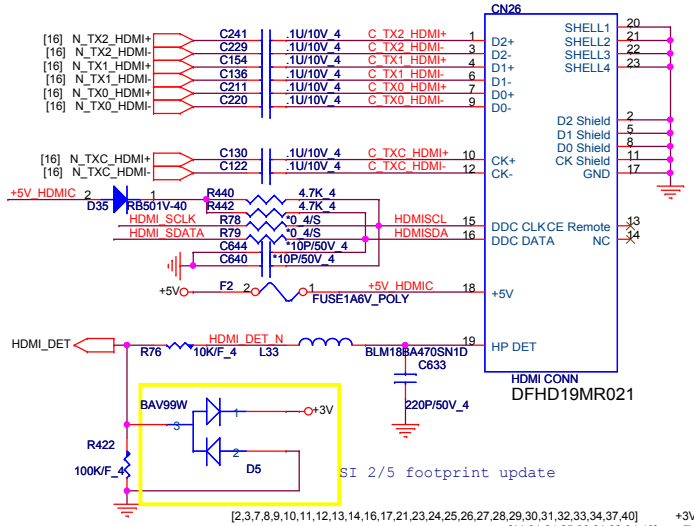


CRT SWITCH



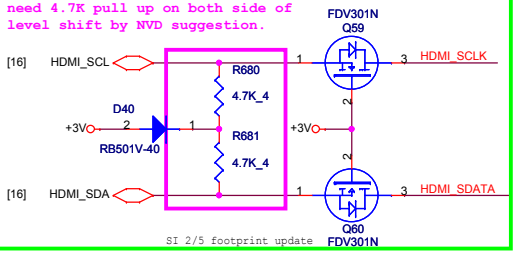
inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

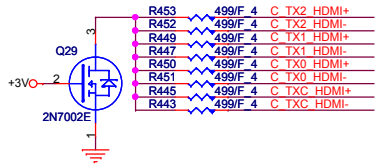
HDMI PORT



11/17 add level shift

03/10 SI changed from 2.2K to 4.7K, DDC need 4.7K pull up on both side of level shift by NVD suggestion.





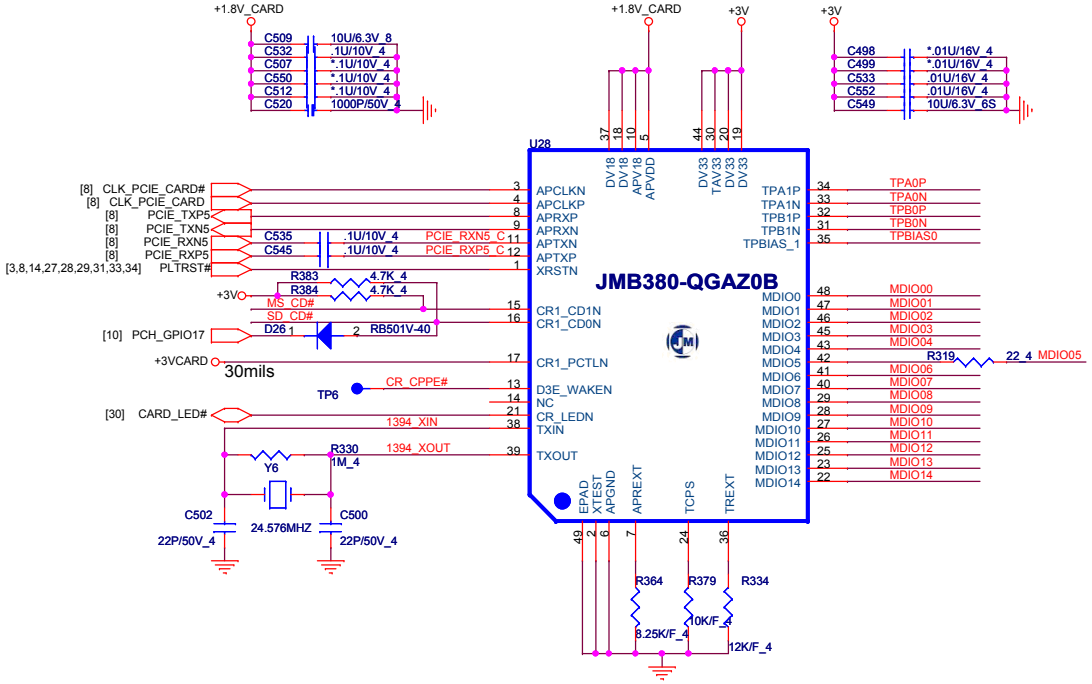
[2,3,7,8,9,10,11,12,13,14,16,17,21,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[11,21,24,25,30,31,32,34,40] +5V

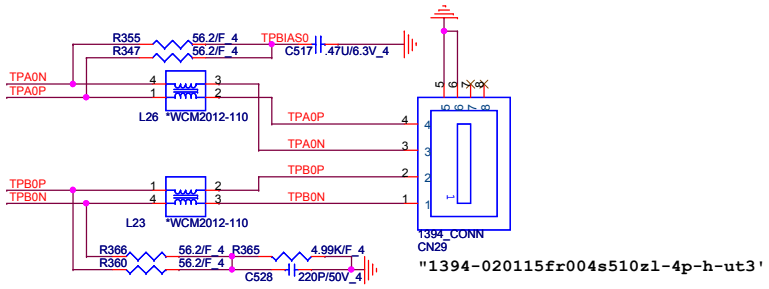
NB5

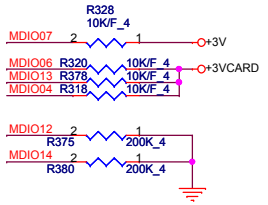
PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	1A

Date: Monday, October 26, 2009 Sheet 22 of 45



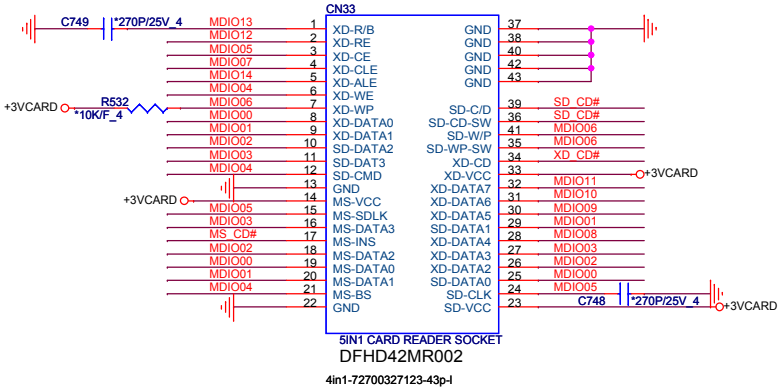


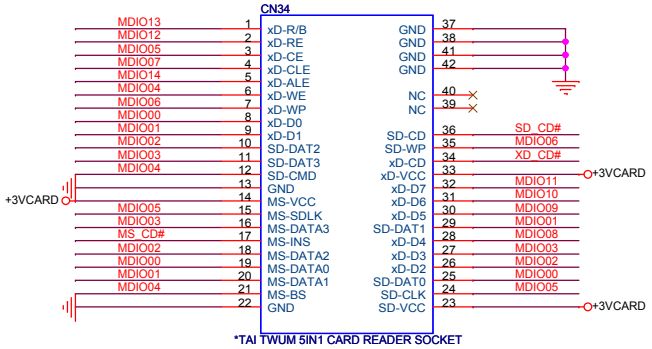


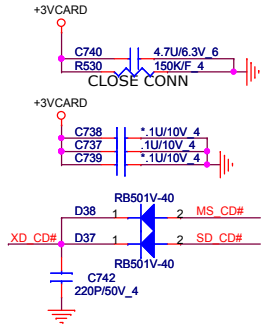
JMB 380 Note:

	SD/MMC	MS	XD
MDIO0	SD_DAT0	MS_D0	XD_D0
MDIO1	SD_DAT1	MS_D1	XD_D1
MDIO2	SD_DAT2	MS_D2	XD_D2
MDIO3	SD_DAT3	MS_D3	XD_D3
MDIO4	SD_CMD	MS_BS	XD_WE#
MDIO5	SD_CLK	MS_SCLK	XD_CE#
MDIO6	SD_WP		XD_WP#
MDIO7			XD_CLE
MDIO8	SD_DAT4		XD_D4
MDIO9	SD_DAT5		XD_D5
MDIO10	SD_DAT6		XD_D6
MDIO11	SD_DAT7		XD_D7
MDIO12			XD_RE#
MDIO13			XD_R/B#
MDIO14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#

5 IN1 CARD READER
XD,MMC/SD,MS/MSP







[2,3,7,8,9,10,11,12,13,14,16,17,21,22,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V

NB5	PROJECT : UP67 Quanta Computer Inc.		
	Size: Custom	Document Number: JMB380 & CR SOCKET	Rev: 1A
	Date: Monday, October 26, 2009	Sheet 23 of 45	

1209 delete R321 for IDT check

Reserve for EAPD#

+3V R329 *5.11K/F_4 EAPD#

Close to Pin9

Close to Pin38

U26 IDT 92HD75B3

TO DOCKING Speakers

TO Audio Jack MIC

TO Internal Speakers and Sub Woofer EQ

TO DOCKING MIC

TO Headphone jack

1209 delete R312 for IDT check

1209 delete C541 for IDT check

For IDT Dolby functionality.

PV modify (PC beep)

HP_EAPD

TPA6040A4	Low enable
TPA6047A4	High enable

Codec	92HD71	92HD75
R571	POP	NA
C716	NA	POP
R449 R510	5.11K	2.49K

5.11K P/N: CS25112FB15

SA_A# -->DOCK HP
SA_B# -->EXT MIC
SB_E# -->DOCK MIC
SA_F# -->EXT HP
Audio JACK: Normal Open

PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

TO AUDIO/B CON.

DFFC12FR293 CN16 AUDIO CONN

EMI 0828

DOCK MIC DETECT

Q26 2N7002E
Q25 MMBT3904-7-F
Q24 MMBT3904-7-F
Q31 MMBT3904-7-F
Q30 2N7002E
Q64 2N7002E

[25,26] +4.75VAVDD
[11,21,22,25,30,31,32,34,40] +5V
[12,25,29,31,35,36,37,38,39,40] +5VPCU
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,25,26,27,28,29,30,31,32,33,34,37,40] +3V

NB5

PROJECT : UP67
Quanta Computer Inc.

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Custom	Azalia 92HD75	1A

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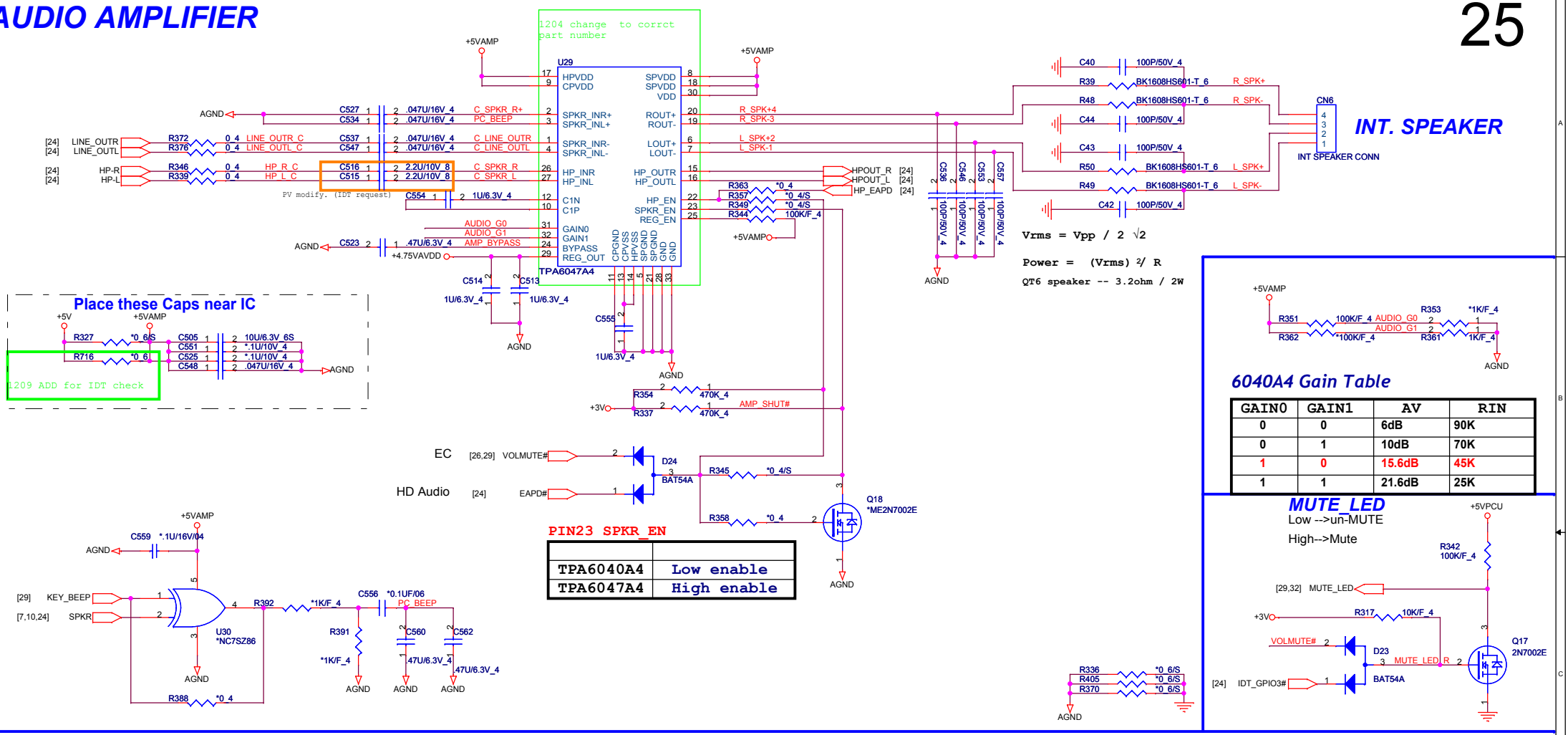
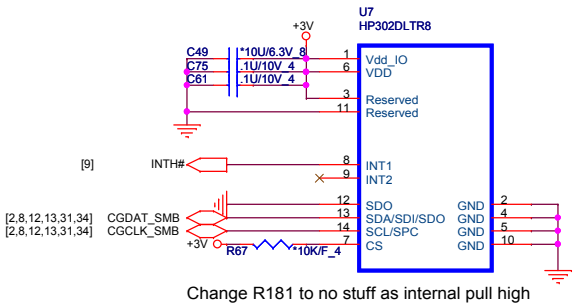
AUDIO AMPLIFIER



Accelerometer Sensor

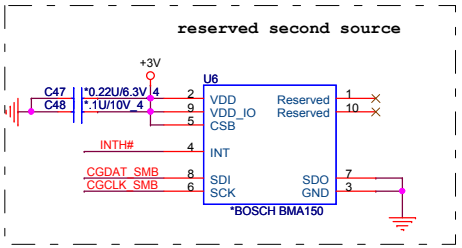
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



Change R181 to no stuff as internal pull high

Pin 12: Low 38hex

Pin 12: unconnected/floating 3Ahex



[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,26,27,28,29,30,31,32,33,34,37,40] +3V
[11,21,22,24,30,31,32,34,40] +5V
[24,26] +4.75VAVDD
[26] +5VAMP

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6047/Accelerometer	1A

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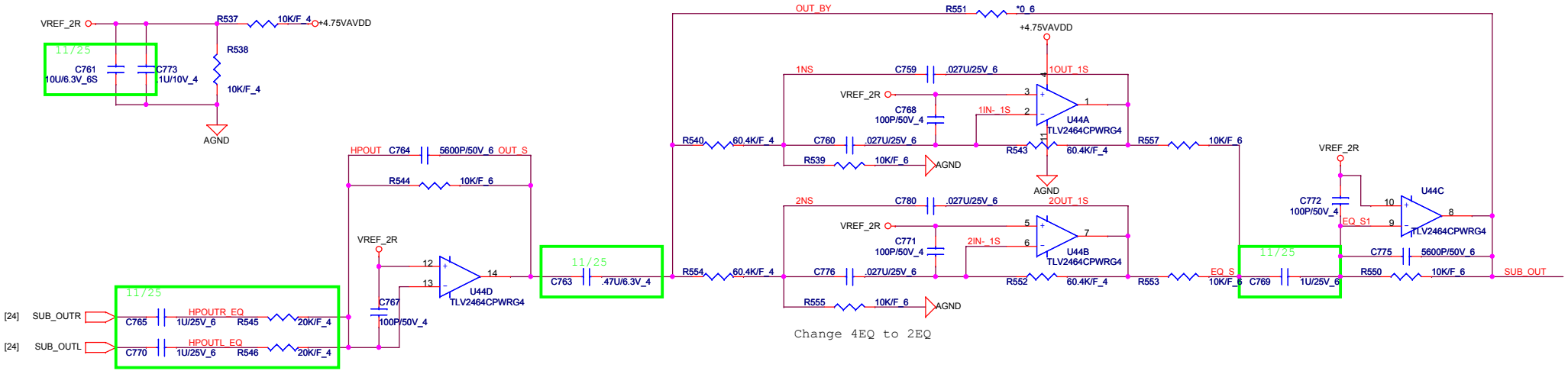
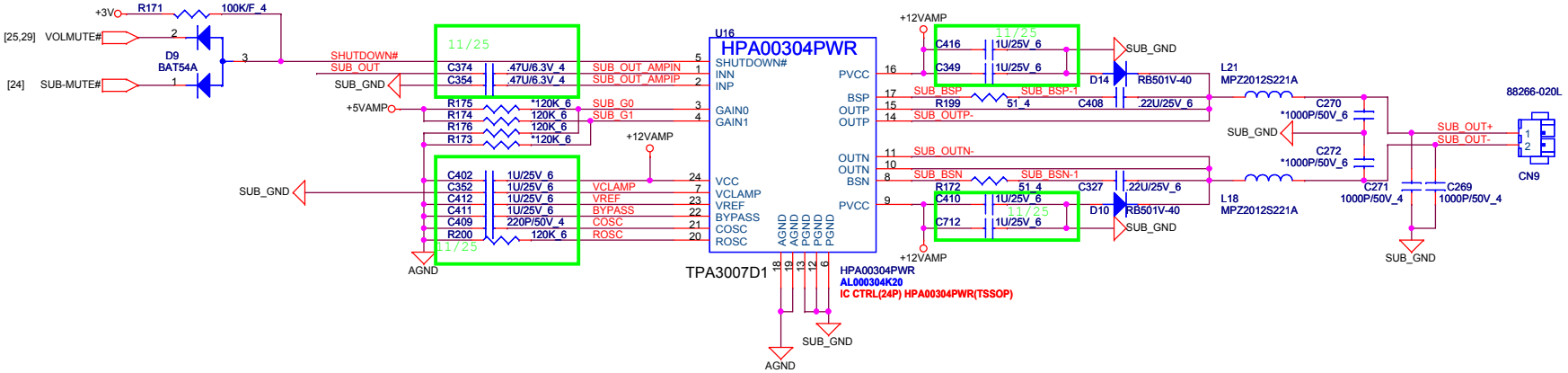
EQ FOR SUBWOOFER

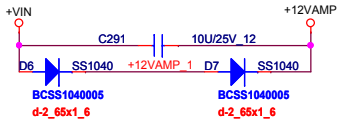


Change 4EQ to 2EQ

MODEL	UP7
R316	60.4K/F_6
R319	60.4K/F_6
R330	60.4K/F_6
R314	60.4K/F_6
C509	0.027U/25V_6
C510	0.027U/25V_6
C529	0.027U/25V_6
C543	0.027U/25V_6



Sub-Woofer power



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

[24,25] +4.75VAVDD
[25] +5VAMP
[21,32,35,36,37,38,39,40,41] +VIN
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,27,28,29,30,31,32,33,34,37,40] +3V

NB5

PROJECT : UP67
Quanta Computer Inc.

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Custom	SUBWOOFER (EQ & AMP.)	1A

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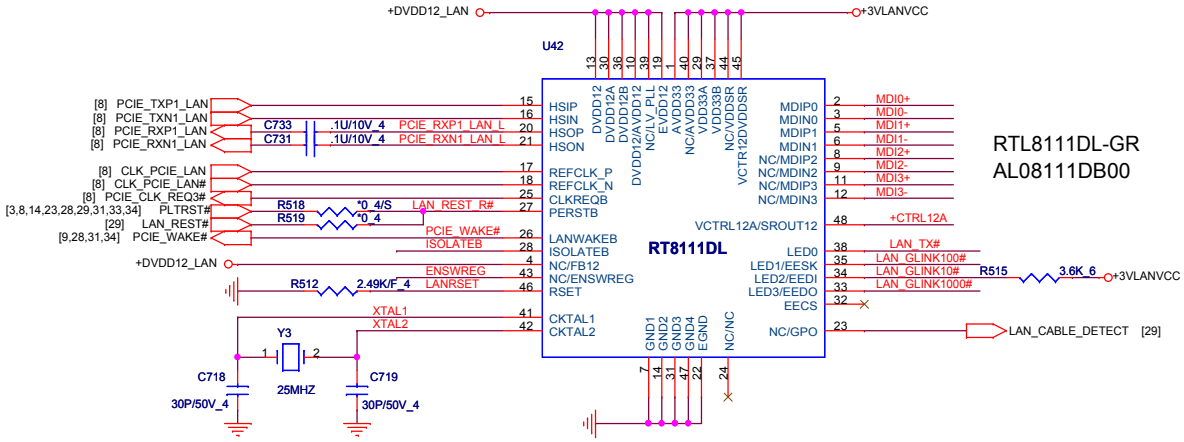
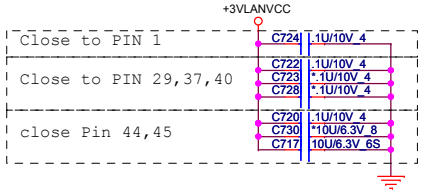
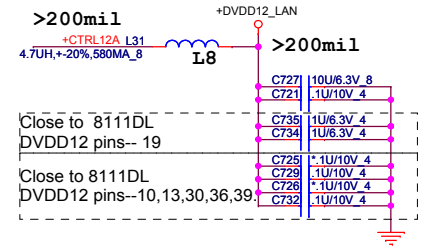
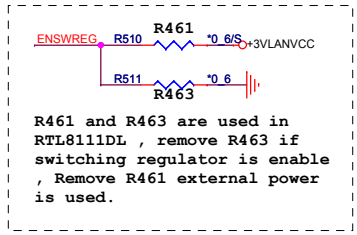
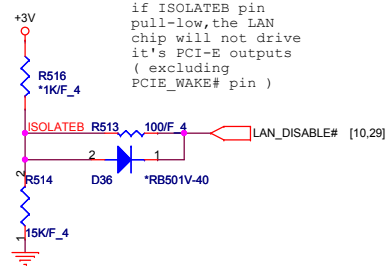


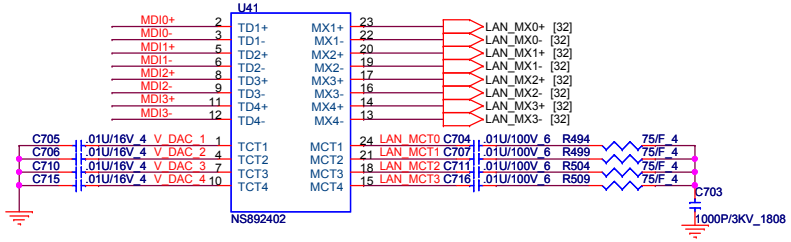




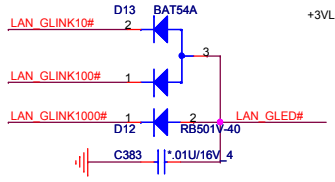


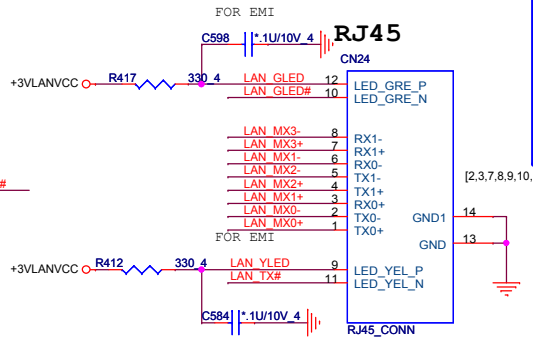


Transformer for 10/100/1000



Lan Con.





NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111DL/8103E/RJ45	1A

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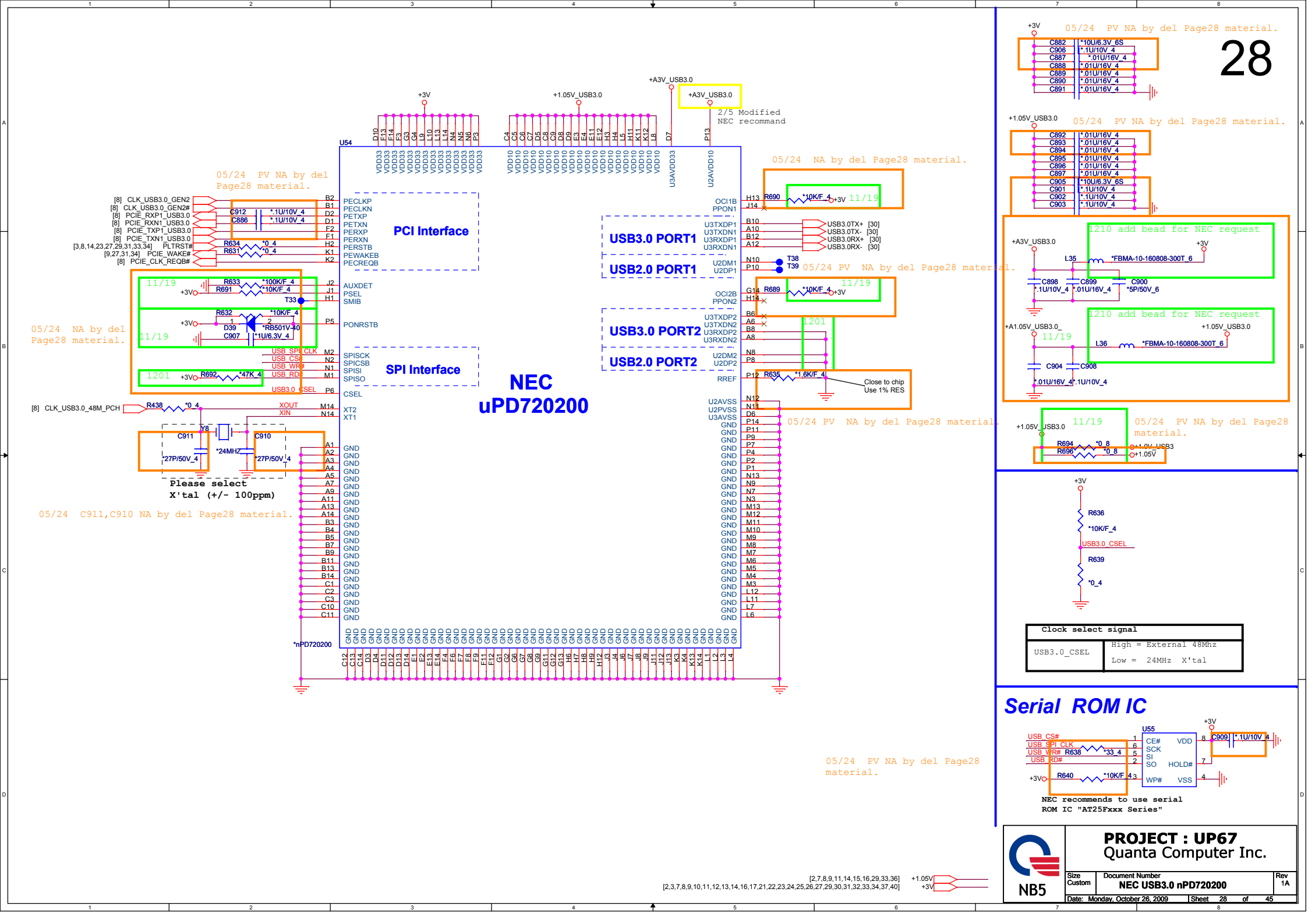
28
NEC
uPD720200
U54
PCI Interface
SPI Interface
USB3.0 PORT1
USB2.0 PORT1
USB3.0 PORT2
USB2.0 PORT2
2/5 Modified
NEC recommand
05/24 PV NA by del Page28 material.
05/24 NA by del Page28 material.
05/24 C911,C910 NA by del Page28 material.
Please select
X'tal (+/- 100ppm)
1210 add bead for NEC request
Close to chip
Use 1% RES
Clock select signal
USB3.0_CSEL
High = External 48Mhz
Low = 24MHz X'tal
Serial ROM IC
NEC recommends to use serial
ROM IC "AT25Fxxx Series"
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Quanta Computer Inc.
NB5
Size Custom
Document Number
NEC USB3.0 nPD720200
Rev 1A
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1212 Change part number to VERSION D2

U23

KB3926QF D2

1208 ADD cpu temp _alert# function

SI 2/5 Modified

For KB3926 B, C version

for EMI

1206 EC add debug pin

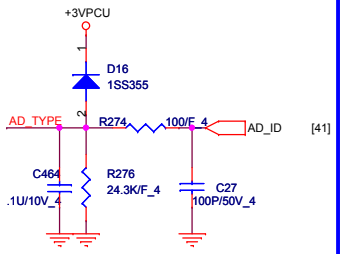
1211 EC add for SMT debug pin

PV modify (Nvidia request)

for Battery charge/charge and cap board

for VGA/CPU thermal

adapter Type check



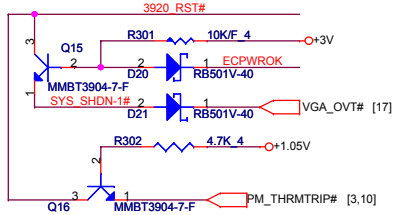
R273

64.9K -->65W CS36492FB17

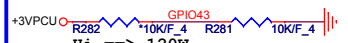
33.2K -->90W CS33322FB13

Change to 1SS355 as Current loss

thermal shutdown circuit



adapter select for EC



Hi ==> 120W

Low ==> 65W/90W

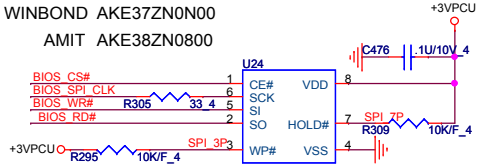
512K byte SPI EC ROM

Socket: DG008000031

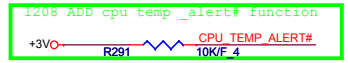
MXIC AKE3KZP0001

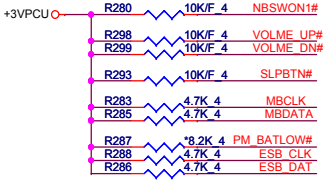
WINBOND AKE37ZN0N00

AMIT AKE38ZN0800

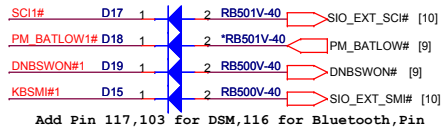


1208 ADD cpu temp _alert# function





Change to RB500 as Current loss



Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier

Delete T10 and tie pin 117 from Lan for DSM

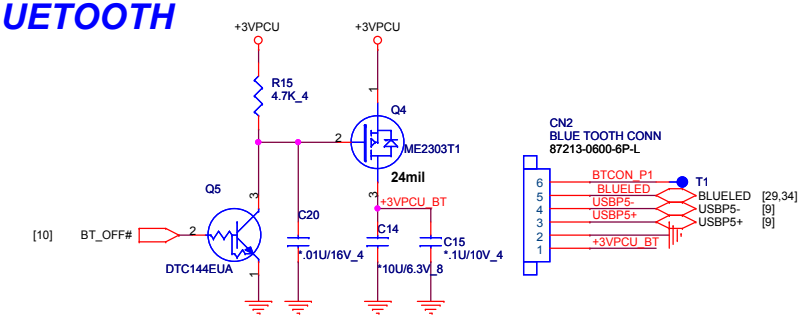
Fan table select

ID	Ra	Rb
UP6	10K	N/A
UP7	N/A	10K

R430 Change to 100k ohm ,pull low

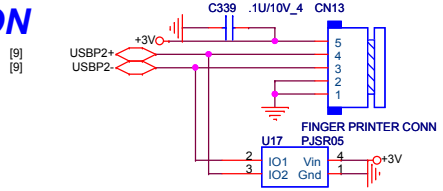
11/6 for EMI

BLUETOOTH

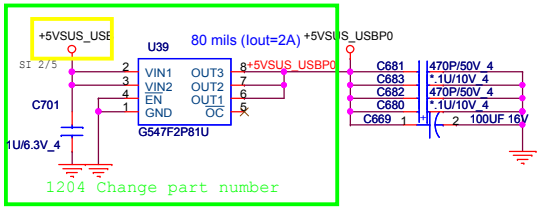


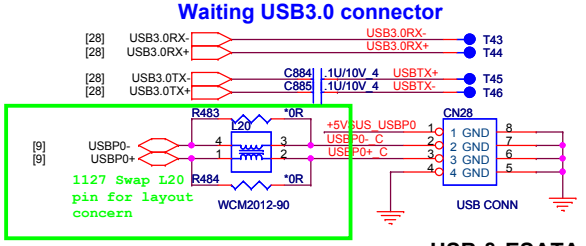
USB fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

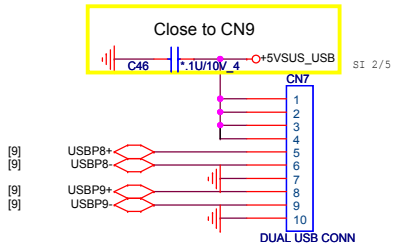


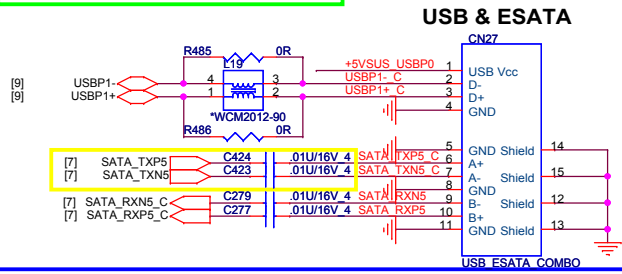
LEFT SIDE USBX1 and E-SATA/USB COMBO



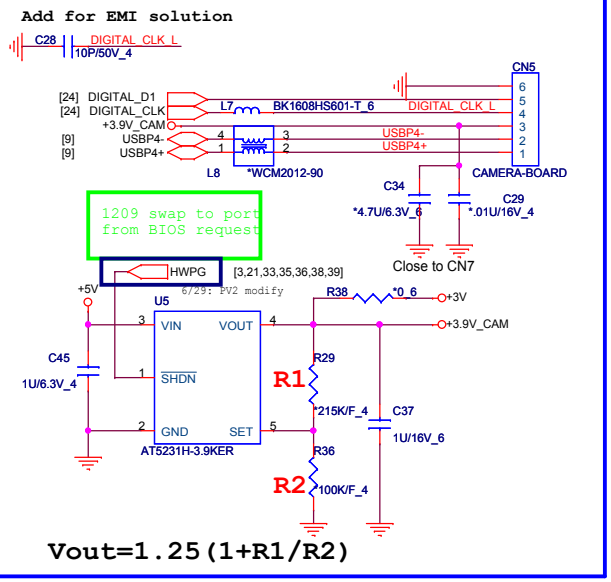


RIGHT SIDE USBX2

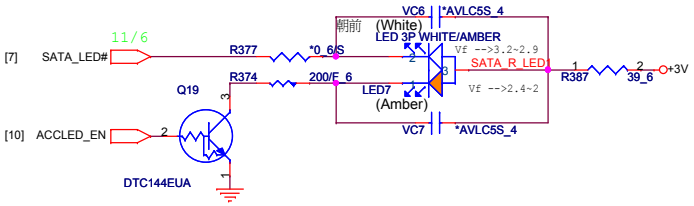


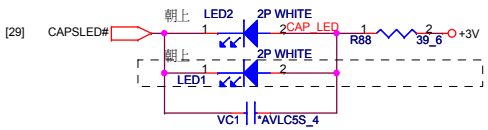


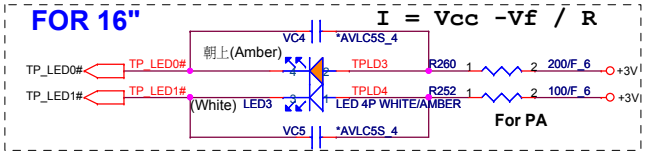
USB CAMERA /DIGITAL MIC CONNECT

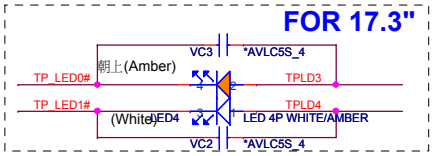


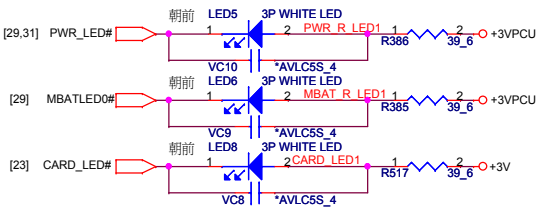
LED



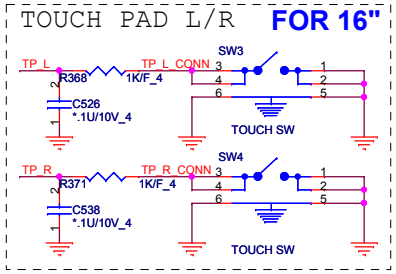


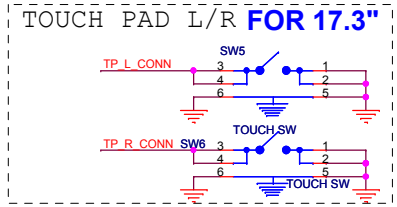


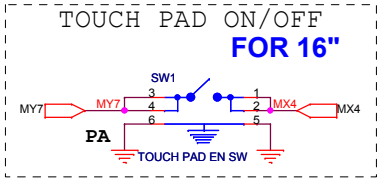


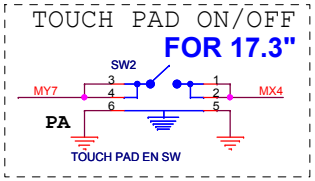


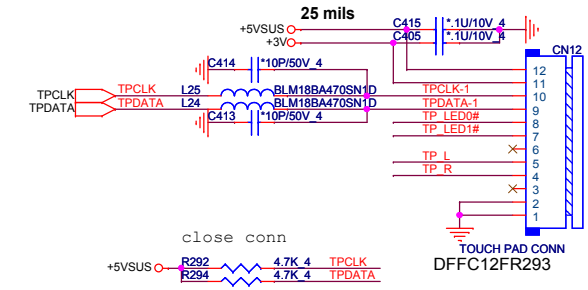
TOUCH PAD CONNECTOR & ON/OFF BOTTOM











[7,12,13,21,29,31,32,34,35,36,38,40,41] +3VPCU
[11,21,22,24,25,31,32,34,40] +5V
[21,32,40] +5VSUS
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,31,32,33,34,37,40] +3V

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WC/FT/ESATA/USB/LED	1A
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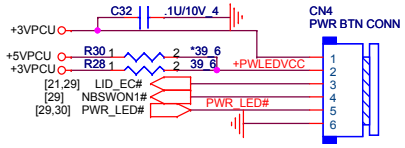
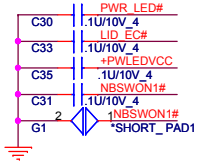
POWER BOTTON CONNECT

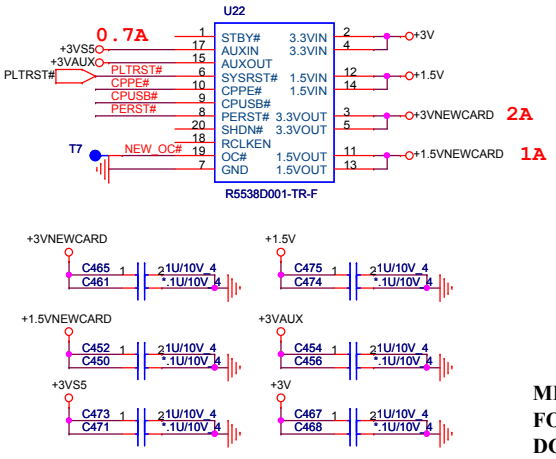


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH [3,8,14,23,27,28,29,34]
4. POWERON#
5. PWRLED#
6. GND

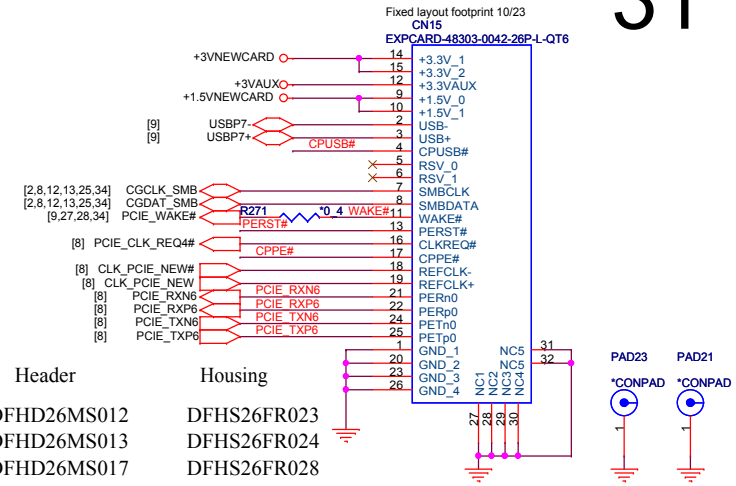


NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)



Fixed layout footprint 10/23

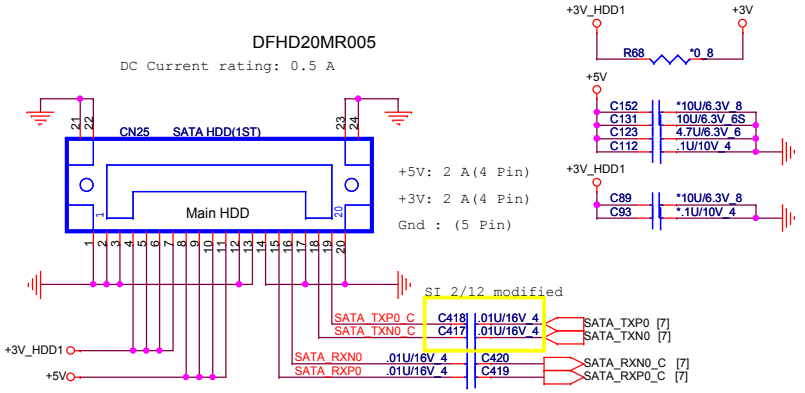


	Header	Housing
MLX	DFHD26MS012	DFHS26FR023
FOX	DFHD26MS013	DFHS26FR024
DGN	DFHD26MS017	DFHS26FR028

SATA HDD CONNECTOR

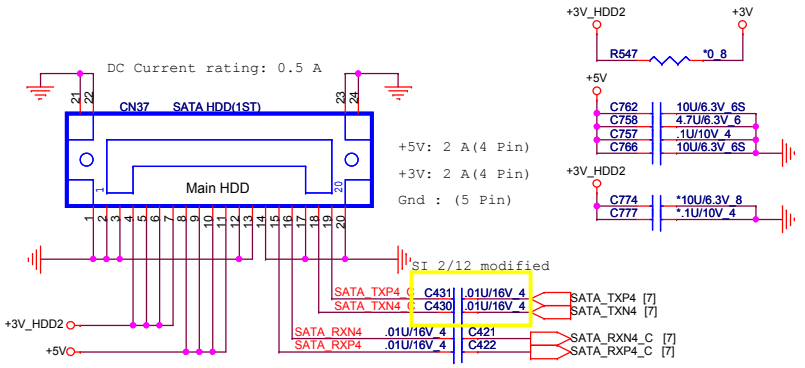
DFHD20MR005

DC Current rating: 0.5 A



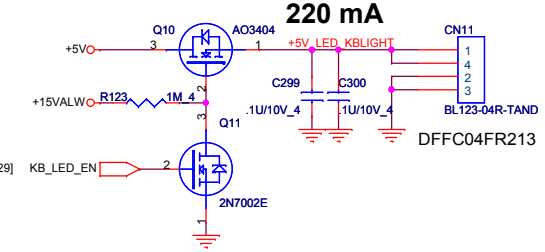
SATA_2 CONNECTOR

DC Current rating: 0.5 A



Backlight Keybaord Con.

220 mA



clear ABS 758 resin for key cap.

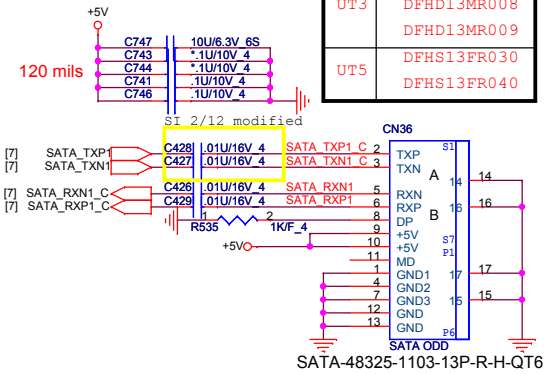
7 LEDs for 15.4" (total LED current 140mA)

11 LEDs for 17" (Total LED current 220mA)

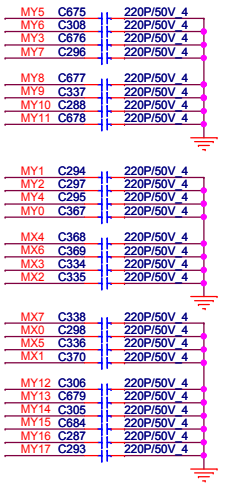
SATA CD-ROM

CN36 part number

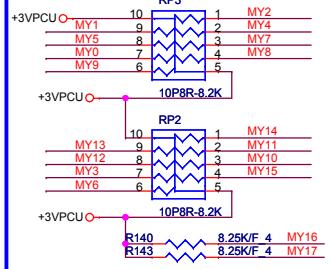
UT3	DFHD13MR006
	DFHD13MR008
	DFHD13MR009
UT5	DFHS13FR030
	DFHS13FR040

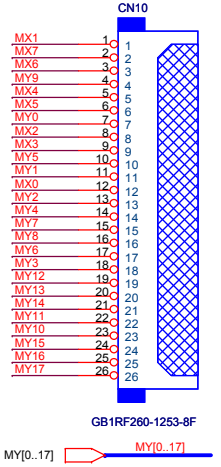


KEYBOARD Con.



KEYBOARD PULL-UP





[15,19,20,34,36,39,40] +1.5V
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,32,33,34,37,40] +3V
[7,12,13,21,29,30,32,34,35,36,38,40,41] +3VPCU
[8,9,10,11,33,40] +3VS5
+3VAUX
[11,21,22,24,25,30,32,34,40] +5V
[21,35,40] +15VALW

NB5

PROJECT : UP67
Quanta Computer Inc.

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Custom	ODD/HDD/NEW CARD/PW/KB	1A
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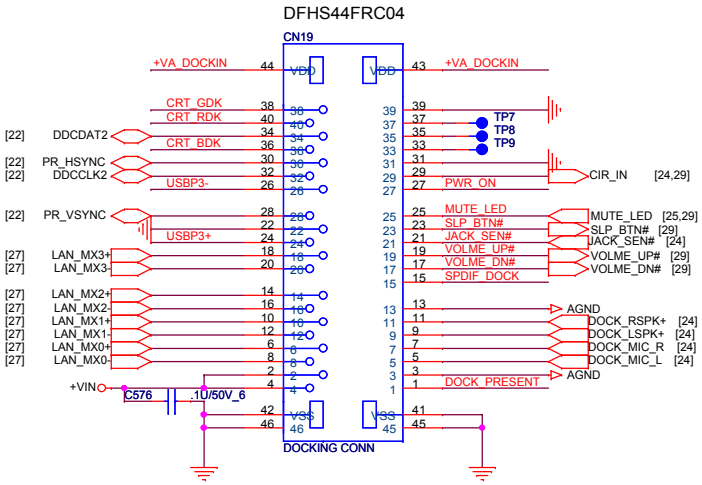
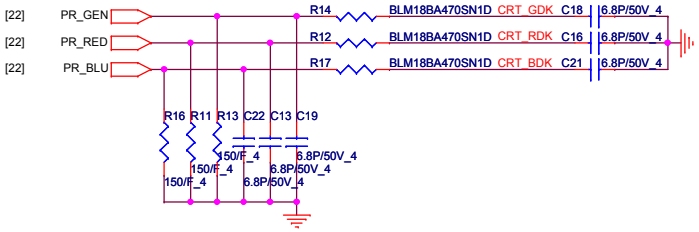
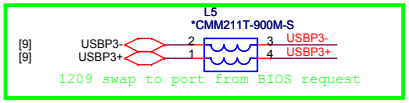
CABLE DOCK

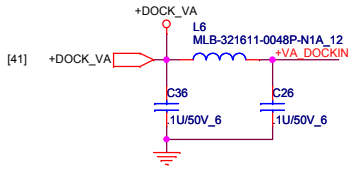


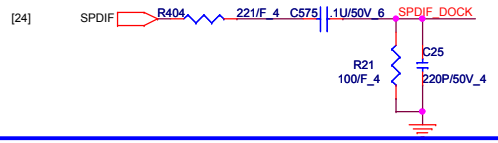
Delete CX08T470000 as CRT rising time and falling time request



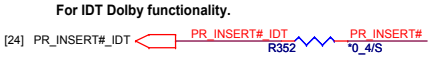


6/1 : PV For EMI request

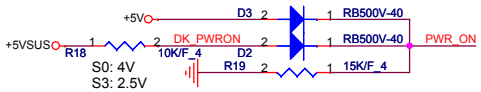


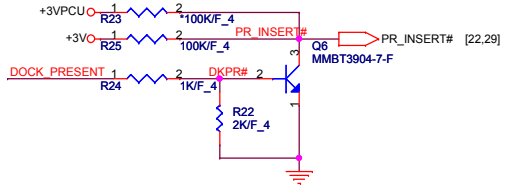


For IDT Dolby functionality.

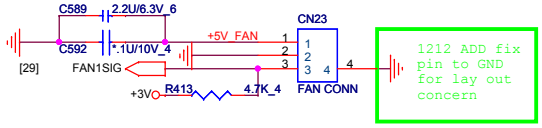


Change to RB500 as Current loss

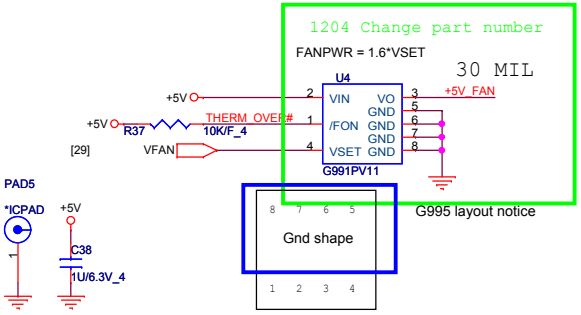




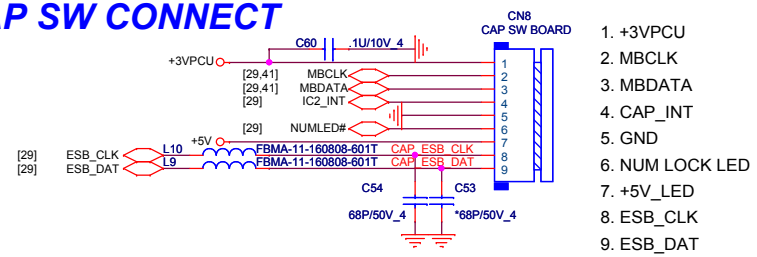
CPU FAN



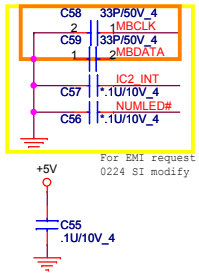
DFHD03MR008



CAP SW CONNECT

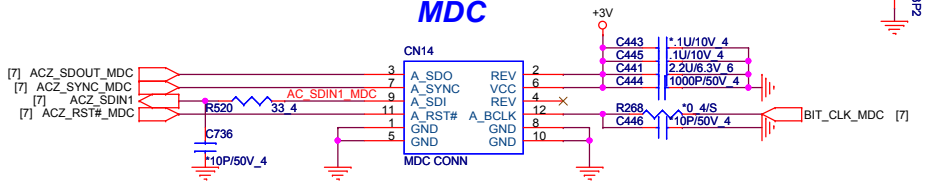


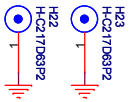
1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT



Modem CONN

MDC





[7,12,13,21,29,30,31,34,35,36,38,40,41] +3VPCU
[11,21,22,24,25,30,31,34,40] +5V
[21,30,40] +5VSUS
[41] +DOCK_VA
[21,26,35,36,37,38,39,40,41] +VIN
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,33,34,37,40] +3V

NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: DOCKING/FAN/CAP/MDC	Rev: 1A
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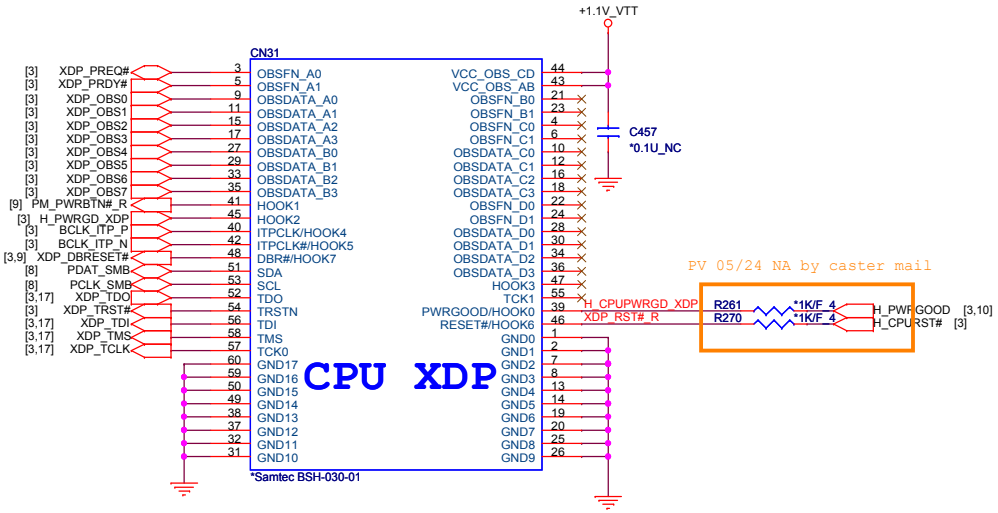
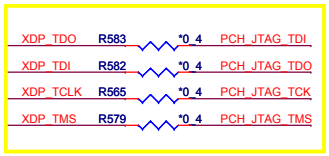
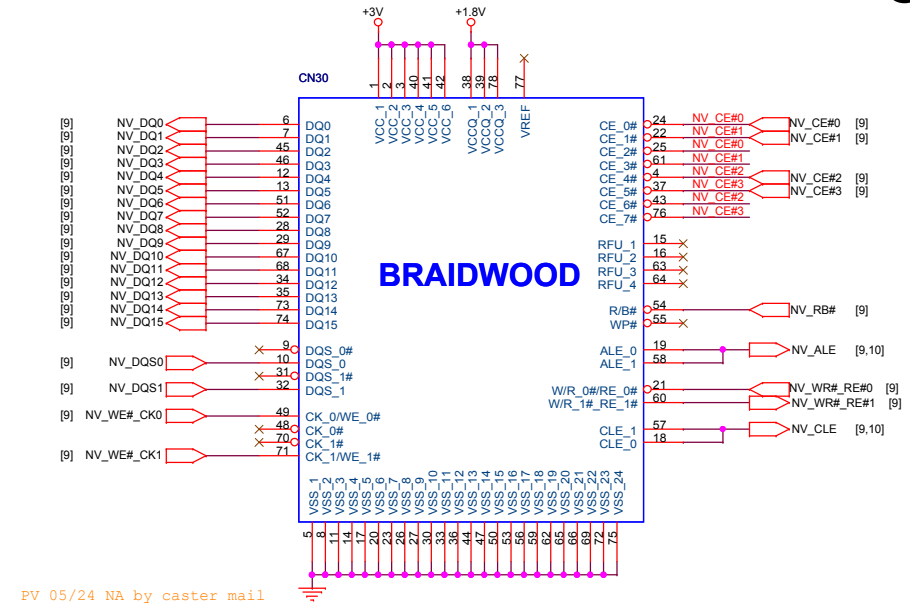
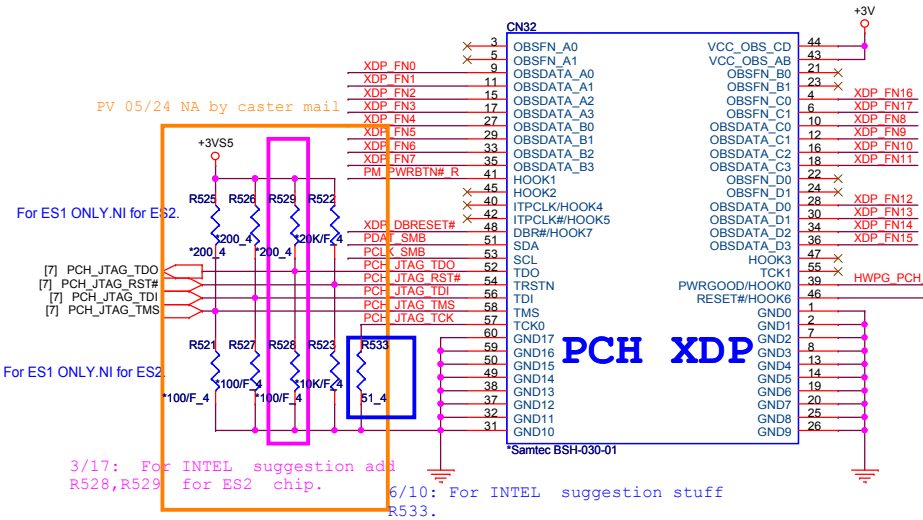
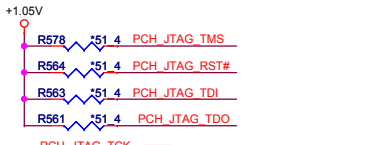


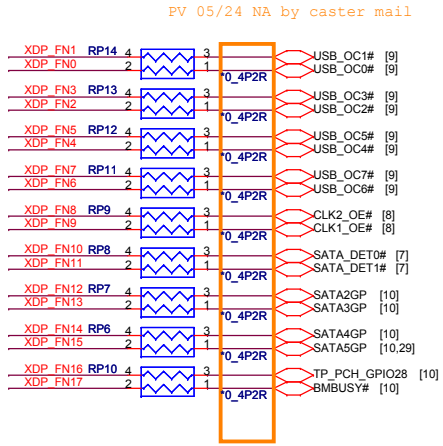
Reserve for BSDL











[3,5,10,11,37,38] +1.1V_VTT
[2,7,8,9,11,14,15,16,28,29,36] +1.05V
[5,10,11,36,40] +1.8V
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,34,37,40] +3V
[8,9,10,11,31,40] +3VS5

NB5

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Quanta Computer Inc.

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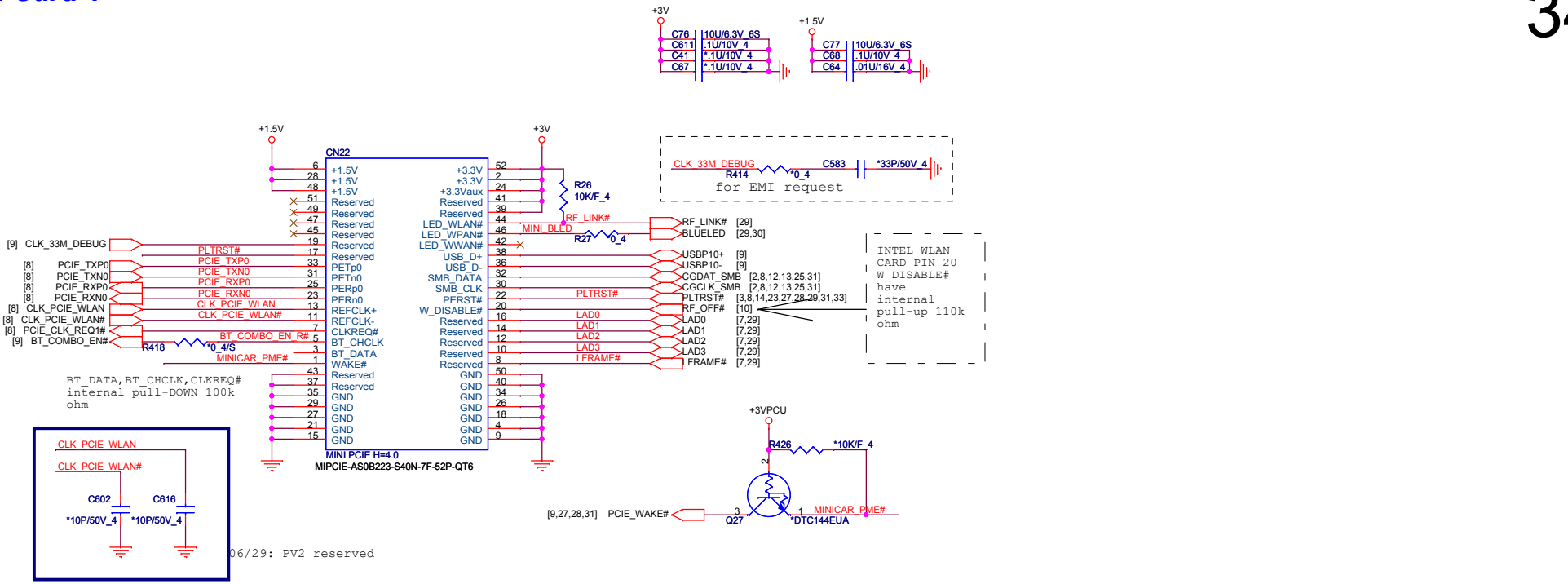
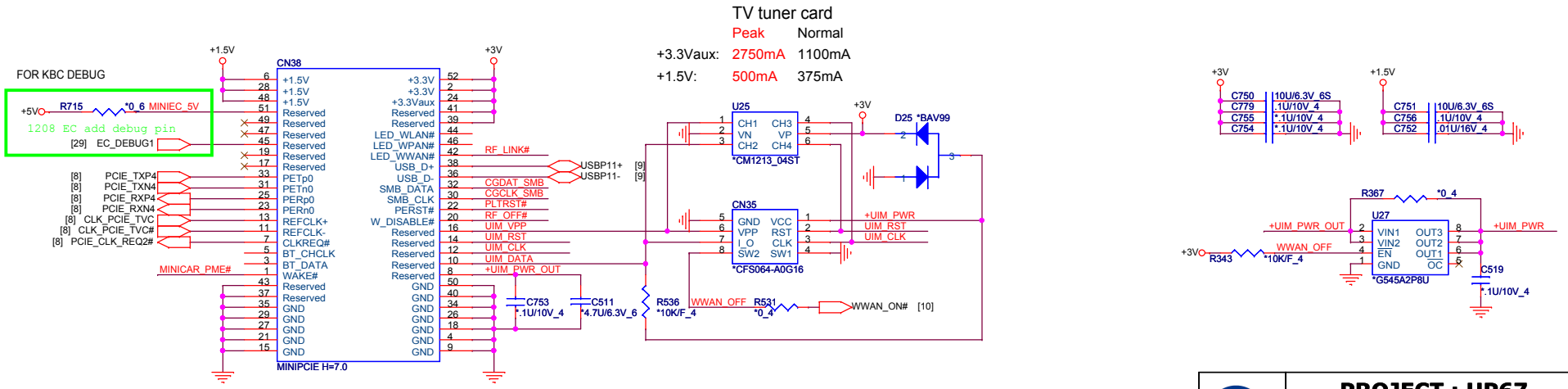
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2 TV Tuner or WWAN



[15,19,20,31,36,39,40] +1.5V
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40] +3V
[7,12,13,21,29,30,31,32,35,36,38,40,41] +3VPCU
[11,21,22,24,25,30,31,32,40] +5V

NB5

PROJECT : UP67
Quanta Computer Inc.

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Custom	MINI PCIE CONN X2	1A

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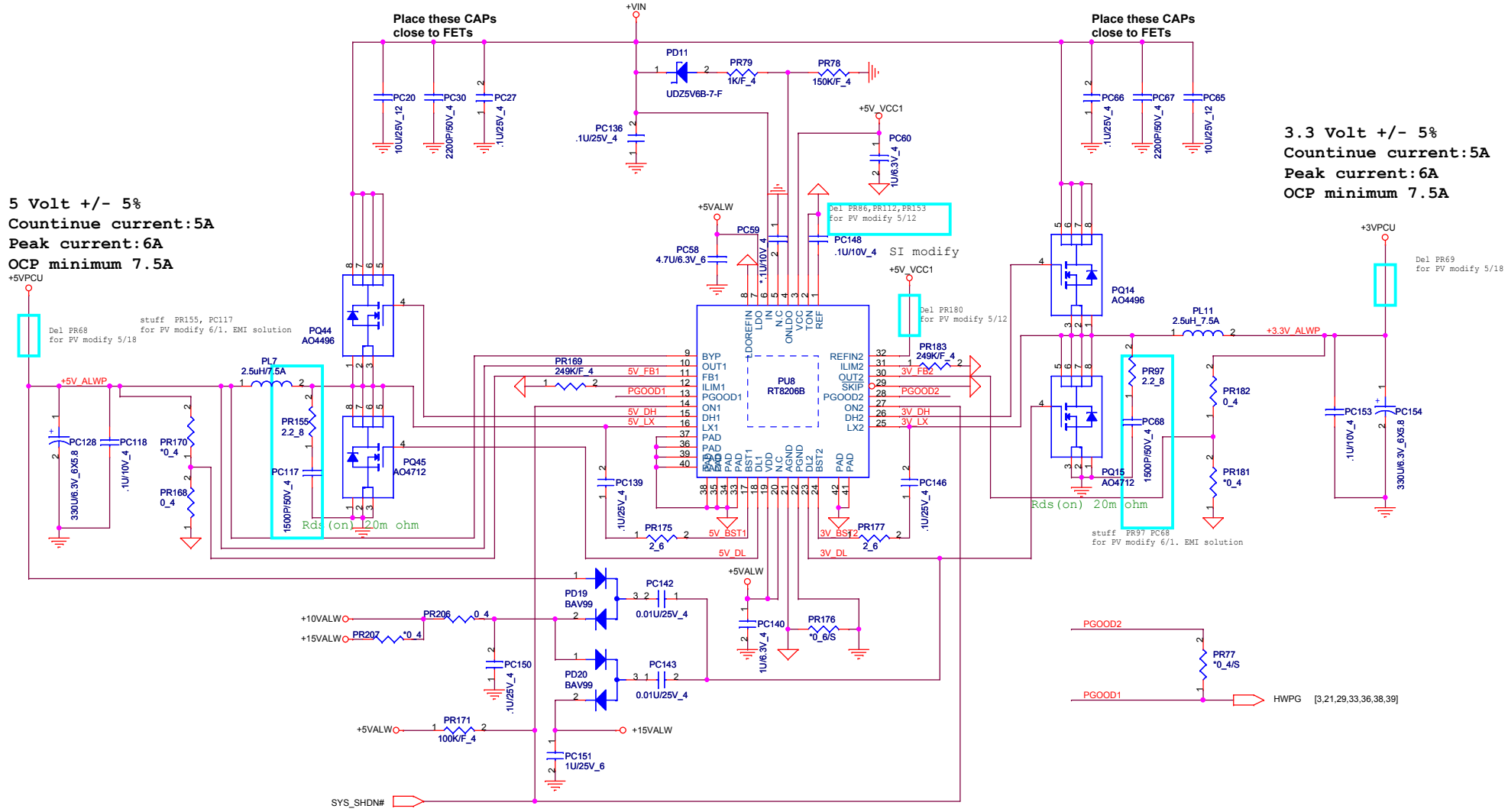
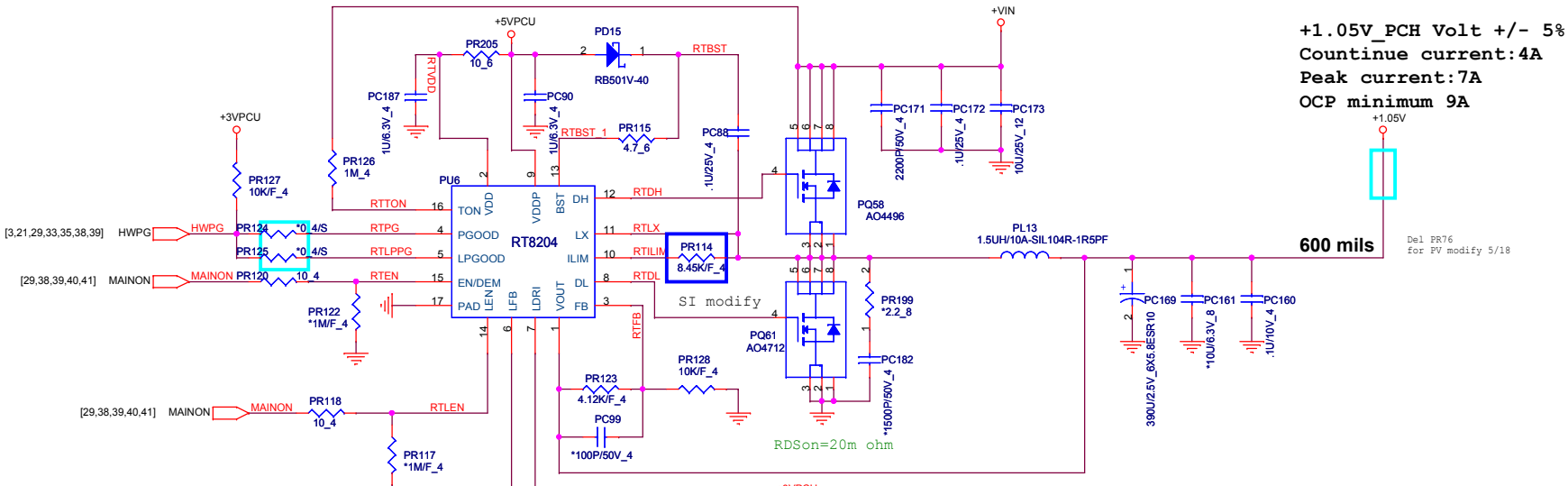
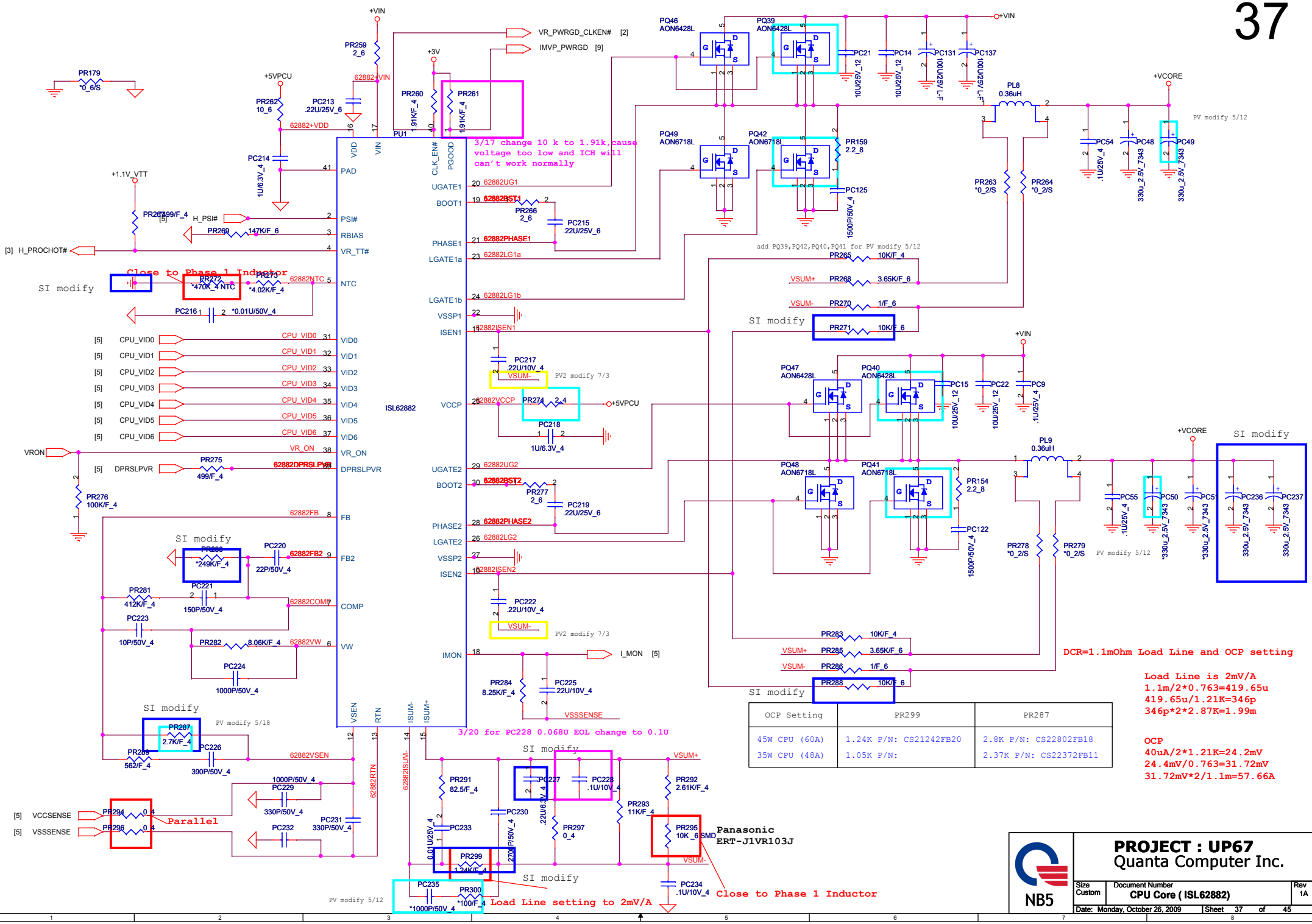
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Monday, October 26, 2009	Sheet 35 of 45	



NB5	PROJECT : UP67 Quanta Computer Inc.		
	Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
	Date: Monday, October 26, 2009	Sheet 36 of 45	


ISL62882
3/17 change 10 k to 1.91k,cause voltage too low and ICH will can't work normally
Close to Phase 1 Inductor
SI modify
PV2 modify 7/3
PV modify 5/18
PV modify 5/12
add PQ39,PQ42,PQ40,PQ41 for PV modify 5/12
3/20 for PC228 0.068U EOL change to 0.1U
Parallel
Load Line setting to 2mV/A
Close to Phase 1 Inductor
Panasonic ERT-J1VR103J
DCR=1.1mOhm Load Line and OCP setting
Load Line is 2mV/A
1.1m/2*0.763=419.65u
419.65u/1.21K=346p
346p*2*2.87K=1.99m
OCP
40uA/2*1.21K=24.2mV
24.4mV/0.763=31.72mV
31.72mV*2/1.1m=57.66A
OCP Setting | PR299 | PR287
45W CPU (60A) | 1.24K P/N: CS21242FB20 | 2.8K P/N: CS22802FB18
35W CPU (48A) | 1.05K P/N: | 2.37K P/N: CS22372FB11
PROJECT : UP67
Quanta Computer Inc.
NB5
CPU Core (ISL62882)
Size Custom
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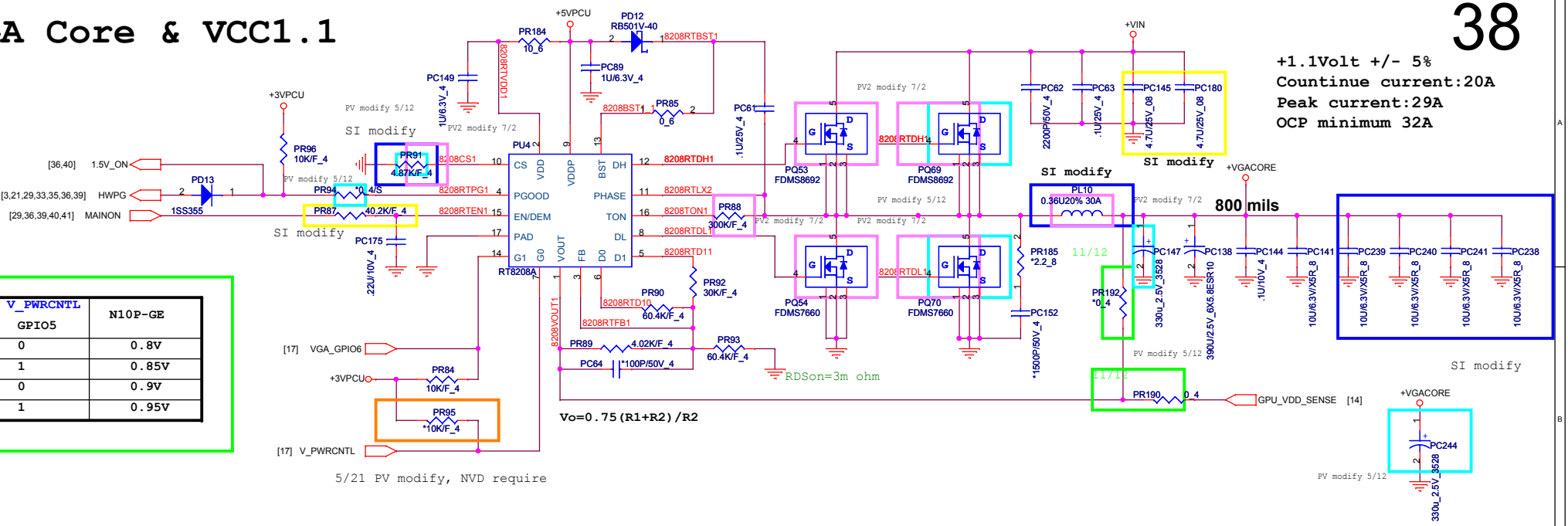
VGA Core & VCC1.1

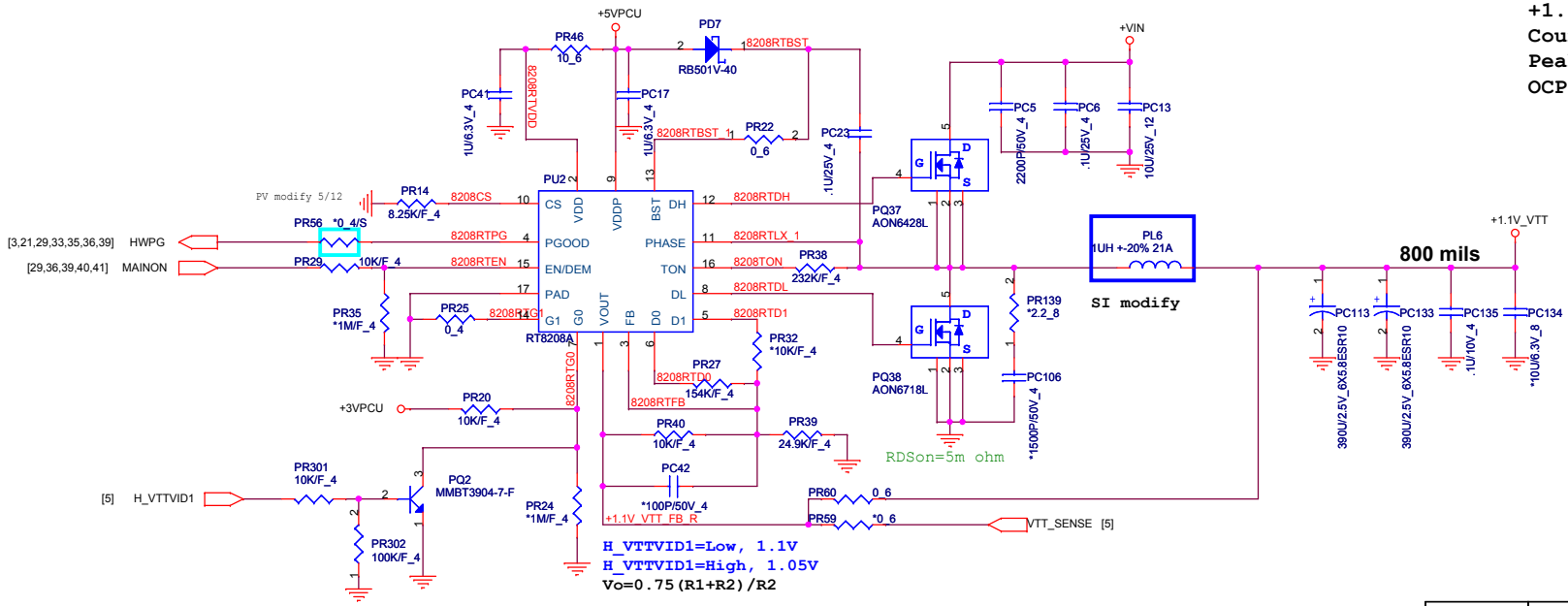
+1.1Volt +/- 5%
Countinue current:20A
Peak current:29A
OCP minimum 32A

11/13

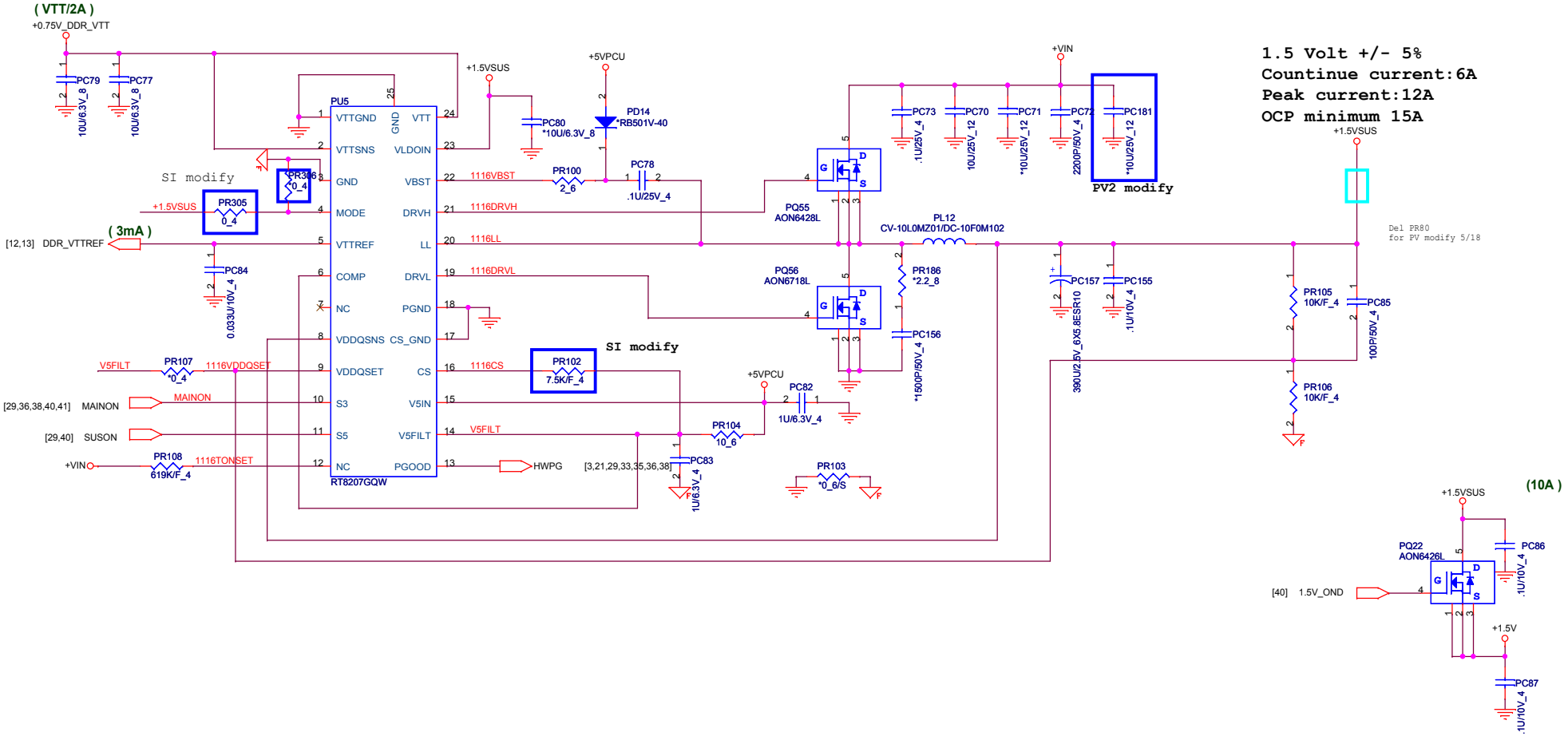
VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5	N10P-GE
0	0	0.8V
0	1	0.85V
1	0	0.9V
1	1	0.95V



+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A



NB5	PROJECT : UP67 Quanta Computer Inc.	
	Size: Custom Document Number: +1.1V_VTT/VGA Core (RT8208)	Rev: 1A
	Date: Monday, October 26, 2009	Sheet 38 of 45



NB5	**PROJECT : UP67** Quanta Computer Inc.	
	Size: Custom Document Number: DDR3 (RT8207)	Rev: 1A
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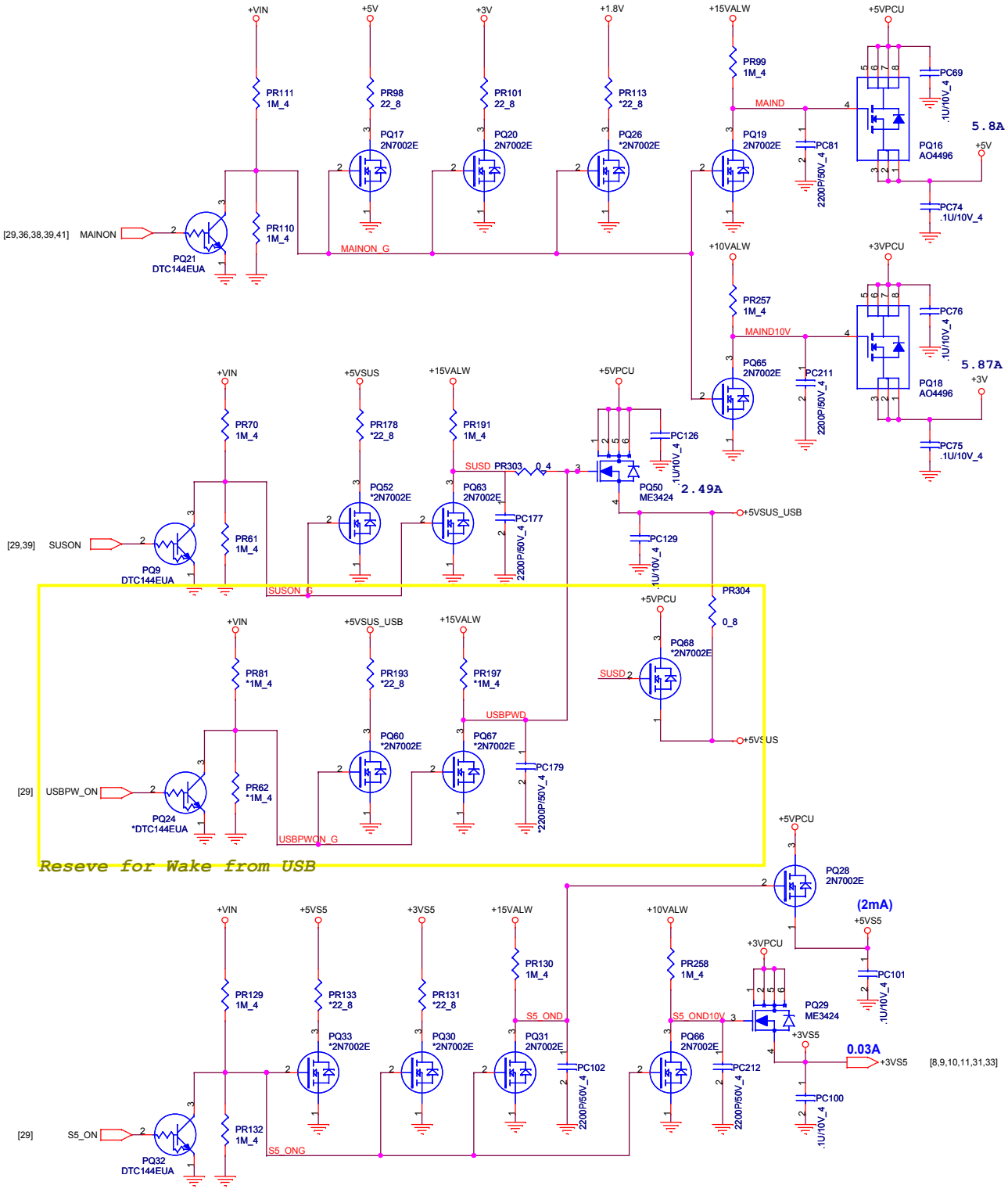

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	1A

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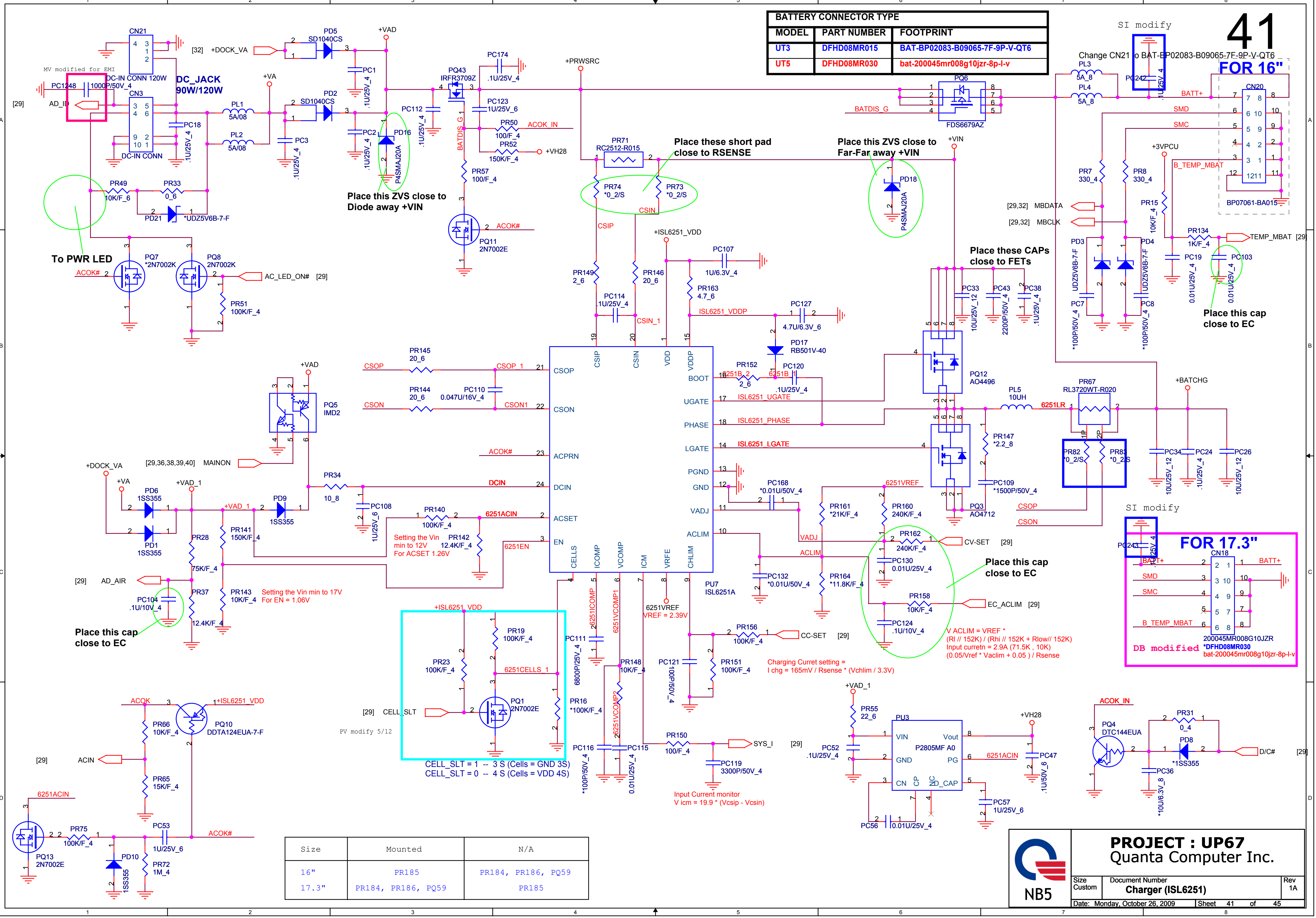

BATTERY CONNECTOR TYPE

MODEL	PART NUMBER	FOOTPRINT
UT3	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT5	DFHD08MR030	bat-200045mr008g10jzr-8p-l-v

Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

NB5

PROJECT : UP67

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (ISL6251)	1A

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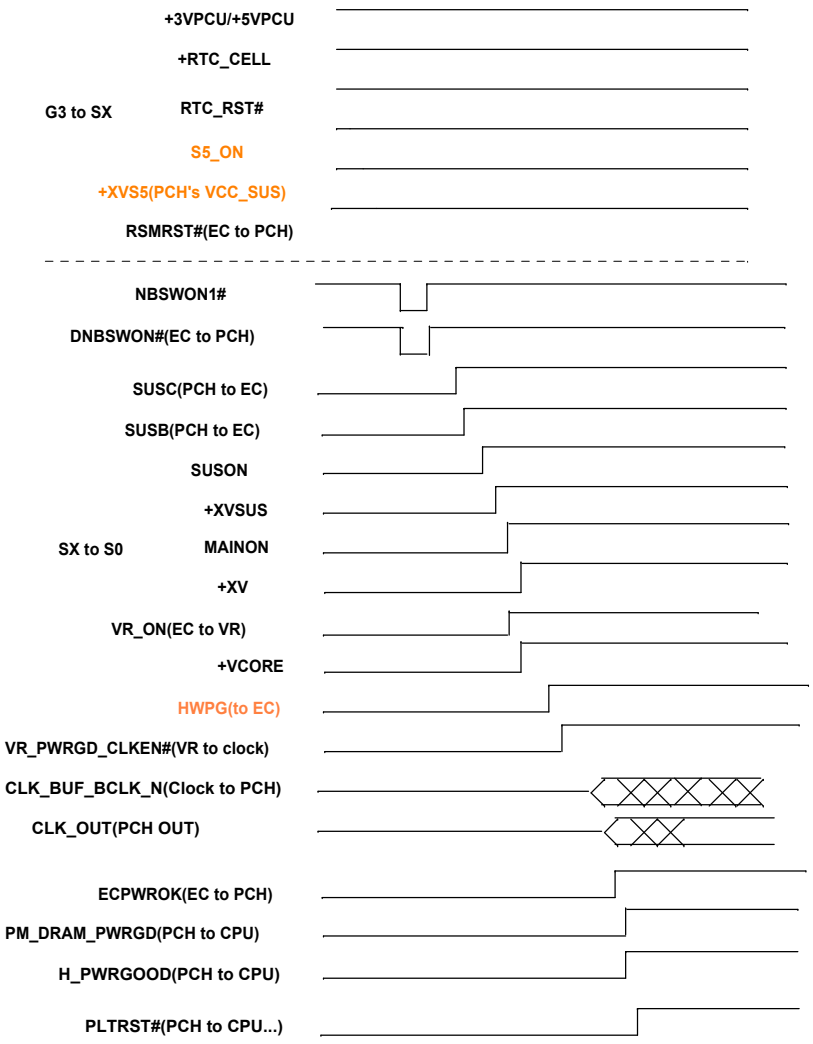
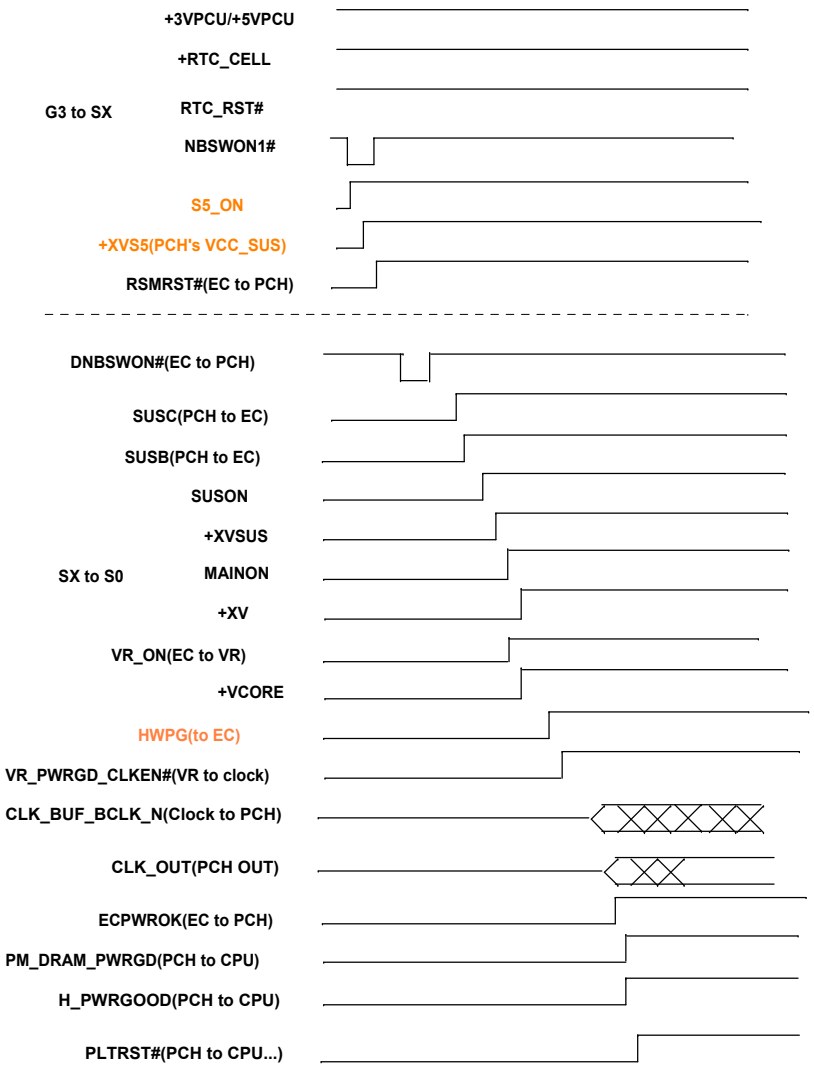
Power up sequence

LAN/RTC WAKE UP ENABLE.



LAN/RTC WAKE UP DISABLE.



NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Power up sequence**	1A

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